CSC Electronics Placement

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CERN TRIDAS Week

- Introduction
- Advantages of Peripheral Mounting
- Data Compression Required
- Resulting Layout
- Challenges
Introduction

• **Old Scheme:**
  - Muon trigger generation by on-chamber cathode and anode trigger “LCT” cards
  - Trigger motherboards on-chamber
  - DAQ motherboards on-chamber

• **New Scheme:**
  - LCT generation, trigger motherboards, and DAQ motherboards in crates on periphery of iron disks
  - Match Track Finder “sector” segmentation: 30° in ME1, 60° in ME2, ME3
Huge Advantages:

- Reduce size of front-end
- Reduce power of front-end
- Reduce complexity of front-end
- Improve access to electronics
- Simplify ME1/1 trigger integration
- Better time scale for trigger cards
- Can move along technology curve ~2 years
- Allow seamless triggering between card boundaries
- Reduce inter-card cabling
- Reduce number of trigger cards
Without compression:

768-960 half-strip cathode bits plus
288-672 wire bits/chamber leads to 40-63
 cables (60-pin) per chamber!

Compression Level 1:

4:1 lossless logic for cathode bits in
 comparator ASIC under development

Compression Level 2:

Lossless 5:1 reduction via high-speed
Channel-Links for cathode and anode

Compression Level 3:

Under discussion for anode data, e.g. :

“Warsaw Compression” almost lossless, x6
 compression with 7-cycle latency (175ns)

Or, exploit preamp deadtime (150ns) to
 multiplex data during “dead time”
Cathode signals - trigger uses half-strip bits

Exploit slow (150ns peaking) cathode signals for 4:1 compression

When signal > threshold and neighbors, encode sequential “triad” bits at 40 MHz:

Bit 1 = Distrip bit
Bits 2&3: Location of half-strip

No additional system latency:
LCT algorithm starts with di-strip bits

Tested in FPGA
Planned for Comparator ASIC #3
National Instruments
“Channel-Links”
meant for laptop LCD displays
Parallel TTL to serial LVDS
40-66 MHz external, 240-304 MHz internal
28 bits on 11 (versus 56) conductors
includes clock regeneration
About $10 = 15CHF per chip
Have tested OK to 8m
on twisted-flat cable @40MHz clock
Additional compression for anode data

CSC anode trigger ~250ns faster than cathode allows time for compression

Scheme proposed for RPC data compression:

Data loss depends on hit rate: 3x10^-6 at 2 kHz/cm², 10^-2 at 4 kHz/cm²

Described at http://cmsdoc.cern.ch/user/p/pozniak/cms/meetings/Agenda_CMS_9711.ps

Prototyped in Altera, ASIC proposed for x6 compression with 7 cycle latency (175 ns)

Another possibility:

Use 150ns deadtime of anode preamp/disc. to send additional data
Front-End Trigger Elements

Cathode LCT:

Anode LCT:

- Discriminators
- Channel Links
- Front FPGAs
- Rear FPGAs
- RAMs
- Data compression
Front-End Layout

Old scheme

New scheme
Each iron disk handles 12 sectors
30° sectors on YE1 for ME1,
60° sectors on YE2 for ME2 and ME3

Per sector:

<table>
<thead>
<tr>
<th>Type</th>
<th>Board</th>
<th>Slots</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLCT</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>ALCT</td>
<td>9</td>
<td>18</td>
</tr>
<tr>
<td>MBT</td>
<td>5</td>
<td>5</td>
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<tr>
<td>MBD</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>MPC</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Total 29 38
Fits two 9U crates

Put crates under catwalk?
Optical Fibers from Front-End?

Engineering advantages...

Reliable data transmission
No length limitation
No ground loops

...Outweighed by cost

Cypress Hotlinks need 2/anode, 6/cathode

About $30 each side.
31392 links = $1884K

HP Glinks need 1/anode, 2/cathode card

At $155 each side
11664 links = $1806K
Challenges

Channel-Link cable length limits:

8 m worked without errors with twisted-flat cable and 40 MHz (Matveev).
Limit depends on clock speed and cables
We will investigate other cables for longer distance, better noise immunity.
We can investigate other chip sets.

CLCT and ALCT card complexity:

More cathode (3-4x) and anode (3-7x) LCT functionality per card is required
9U boards are 2.5x bigger than LCT cards
We are investigating simplified algorithms, on-FPGA lookup tables, and better router