TMB Status

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Topics:

• TMB hardware
• TMB firmware
• TMB testing
• Virtex-II mezzanine card for future
• Lemo cables
• TMB2001 prototypes for use at FAST sites and for system tests
• Produces cathode patterns from comparator outputs
• Correlates cathode and anode (from ALCT) patterns
• Sends chamber-level trigger decision to MPC
• Raw hits data “spooled” to DMB
• Interfaces to “everything”
  • CFEBs
  • DMB
  • CCB
  • ALCT
  • MPC
  • VME
  • RPC (later)
  • JTAG
TMB Hardware Status

• 17 TMB boards were produced (all FAST sites plus development uses)

• Bad job done by assembly company:
  • Connectors soldered in crooked, boards could not be inserted
  • Connectors were removed and reinstalled properly by UCLA
  • Misc. errors (about seven per board)

• 2 boards have been fully corrected and debugged, including CFEB, ALCT, DMB, DDU, CCB interfaces

• 1 TMB ships today to OSU for CFEB/DMB/DDU tests, will be shipped on to Florida

• The other TMB is for continued firmware development at UCLA

• About 2 dedicated days/board to debug the remaining TMB prototypes
TMB Firmware Status

- All interfaces defined (VME, ALCT, CFEB, CCB, DMB, MPC) and mostly debugged
- Features:
  - VME registers (62 x 16 bits) for configuration, including re-configuration of Eproms and FPGAs on TMB and ALCT
  - Automatic boot-up in default configuration
  - Fake CCB section for self-testing
  - ALCT and CLCT test pattern injectors (no ALCT board required)
  - PHOS4 power-on sequence work-around allows board to operate
    - Wait 1 second, send a reset, wait 1 second, program via I2C bus
    - (Previously, PHOS4 chips did not power up in clocking state (dead board!), 5ns delay sometimes became 10ns etc.)
    - Still have very asymmetric (58/42%) output clock
• **Internal tests:**
  - Logic all simulated in Foundation
  - VME register I/O and functionality tested
  - Internal pattern injector tests:
    - CLCT logic works
    - CLCT raw hits readout works
    - ALCT raw hits spooler works
    - TMB coincidence logic works
    - (MPC logic not fully tested)

• **External loop-back testing of all I/O signals**
ALCT-TMB Testing
TMB-CFEB-LVDB Test
TMB Testing II

• Tested with ALCT using delay-chip patterns (see trigger and DAQ output)
  • 80 MHz mux/de-mux works
  • Single clock gives 8 ns window (out of 12 ns possible) for correct data transfer (permanently timed in, independent of cable length)
  • Tx and Rx data checked
  • ALCT-TMB trigger pipeline could not be timed in yet (no ALCT external trigger)

• Tested with single CFEB
  • Adjusted CFEB clock phasing so 80 MHz arrives correctly
  • Perfect results using TMB crystal oscillator
  • Use of CCB PHOS4 gives asymmetric clocking and sometimes requires power cycling. (Improved by replacement of a buffer chip on CCB.)
Using DYNATEM to communicate from a Linux PC to the VME crate.

New software has been written to control TMB functions using socket connections. Needs to be improved. (OSU)

Maybe it is necessary to agree to one protocol (?)

Injected patterns into the delay lines of the ALCT using self triggering. injected patterns into the CFEBs.

Found maybe problems with the PHOS4-chips again. CCB uses them for delaying the clocks.

Looked at the results on TMB side. It depended on how the CCB PHOS4-chips powered up in respect to the TMB PHOS4-chips.

Next step is to write the software to decode the data coming to the TMB from ALCT and CFEB and check the data. (OSU?)
Still to do at UCLA and OSU:

- Decide if clock symmetry needs CCB or CCB+TMB fix (e.g. jumper out PHOS4 delays)
- Check DMB clock delay
- External trigger CCB+TMB+DMB, read out DMB/DDU
- Prepare Dynatem software

At Florida (or UCLA) FAST site:

- Integrate anode and cathode LCT and raw hits readout into FAST site setup
- Verify system operation with various internal and external trigger modes
Virtex-II Mezzanine Card

- **Possibility of Virtex-II on mezzanine card:**
  - Allows better capacity/cost, and higher maximum capacity
  - Different (better?) SEU characteristics
  - Requires ~2 months additional engineering to do layout
  - Higher speed is attractive for final TMB (e.g. ~50 -> ~80 MHz)

- **Drawbacks:**
  - no flexibility in chip selection (E-series layout handles 600E through 2000E chips).
  - Requires 1.5v core voltage (different LVDB resistor choice)
  - Very high density: for instance, where to put power filter capacitors?

- **Can save on FPGA costs (~500 units TMB, maybe ~500 ALCT):**

<table>
<thead>
<tr>
<th>Virtex-E chip</th>
<th>Price</th>
<th>Virtex-2 equivalent</th>
<th>Price</th>
<th>Savings @500 units</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCV600E-7FG680C</td>
<td>$600</td>
<td>XC2V1000-5FF896CES</td>
<td>&lt;$532</td>
<td>&gt;$34K</td>
</tr>
<tr>
<td>XCV1000E-7FG680C</td>
<td>$1193</td>
<td>(XC2V3000-4BG728CES)</td>
<td>(&lt;$1142</td>
<td>&gt;$25K</td>
</tr>
<tr>
<td>XCV1600E-7FG680C</td>
<td>$1843</td>
<td>XC2V3000-4BG728CES</td>
<td>&lt;$1142</td>
<td>&gt;$350K</td>
</tr>
<tr>
<td>XCV2000E-7FG680C</td>
<td>$2865</td>
<td>XC2V3000-4BG728CES</td>
<td>&lt;$1142</td>
<td>&gt;$862K</td>
</tr>
</tbody>
</table>
Virtex-II Mezzanine Initial Layout

- Designed for “medium” (896 ball) FPGAs for TMB (or ALCT)
  - XC2V1000, 1500, 2000 chips
- Compatible size, mounting, and connectors (different core voltage)
- Ball locations compatible with “large” (1152 ball) FPGAs for e.g. Sector Processor
  - XC2V3000, 4000, 6000, 8000, 10000 chips
- Layout by Kan (PNPI), compatibility idea from Matveev
Test Pulse Lemo Cables

• Received all parts:
  • 16000 ft of non-halogen cables
  • 5000 lemo connectors
  • Labels
  • Crimp tool

• Prototype bundle of 6 evaluated:
  • Inward direction of Lemo connectors on ALCT required for ME1/2 integration
  • Outward direction would be better:
    • Some interference with AFEB connector ground lugs
    • Some exposed vias on ALCT boards near the cables could possibly short to lemo connector (now covered with tape)