ALCT and TMB Status

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Topics:
- ALCT2001-384(a) prototypes (6)
- ALCT2001-384(b) pre-production (30)
- Delay ASIC agreement with CMU
- ALCT testing
- Mezzanine cards and FPGAs
- TMB2001 Status
- ALCT672
- Lemo cables
- ALCT database
- Use of CLCT pattern in descoped ME1a
• 6 base boards were produced August 2001
• 14 mezzanine boards assembled
• Bench and cosmic ray (+source) performance is good
• Cosmic ray testing continues
• Did 2 radiation tests (1st w/XCV1000E, 2nd w/XCV600E)
• Radiation resistance: ~1/5 the SEU rate plus 4x faster reloading -> 20x less deadtime for CMS reloading.
• Reliability is good but not perfect
  • Need to work with assembler to reduce solder errors (typically 6 per base board, <1 per mezzanine board)
  • Some BGA connections lost: treatment of mezzanine card (e.g. gold immersion or white tin methods) should help
• Only modest technical improvements are needed
Changes from ALCT2001 to ALCT2001b

Mechanical:
- Add bolts to hold mezzanine card to ALCT base card.
- Move jumpers and test points out from underneath mezz card, move vias out from under mezz stiffener plate.

Electrical:
- Rad-tolerant regulator.
- Fix power-on latch-up problem.
- Reduce number of buffers used in clock distribution (minimize skew).
- More precise thresholds and power voltage readings (ADCs and DACs).
- Change values of capacitors on mezzanine card for optimum high-frequency filtering.
- Add place for power-up holdoff chip for when used without TMB hard reset control (e.g. for Muon Port Card).
- Fix board ID chip layout.
- Add some test points, add clear labels, change power LEDs from green to red (so 1.8v LED will light up).

ALCT passed ESR review at CERN last December 3
• Batch of 30 bare boards received
• 11 assembled boards tested
• Still assembly problems – hairline shorts
• 12 more boards shipped yesterday from assembler
Mezzanine Cards and FPGAs

- 70 bare mezzanine cards produced (also used for TMB, MPC)
- Gold immersion surface treatment much better than previous (flatter)
- 100 Xilinx XCV600E-7FG680C received, also Eeproms and other parts
- Should ship next week to assembler
Delay ASICs

Produced and tested by Carnegie-Mellon
Chips in production testing phase
Delay slope varies substantially
At code=15 (max delay), data bins:

1. 42 ns - 25 chips 1.6 ns/div "road" = 3.3 ns
2. 44 ns - 85 chips 1.7 ns/div "road" = 4.8 ns
3. 46 ns - 150 chips 1.8 ns/div "road" = 4.3 ns
4. 48 ns - 185 chips 1.9 ns/div "road" = 4.5 ns
5. 50 ns - 290 chips 2.0 ns/div "road" = 4.8 ns
6. 52 ns - 330 chips 2.1 ns/div "road" = 4.7 ns
7. 54 ns - 586 chips 2.2 ns/div "road" = 4.7 ns
8. 56 ns - 373 chips 2.3 ns/div "road" = 4.5 ns
9. 58 ns - 99 chips 2.4 ns/div "road" = 4.3 ns

Use “bins” 3-8 only (45-57 ns)
Actual slope set by external resistor
Different resistor choices for ALCT-384/672/288 to equalize somewhat
First Delay ASICs shipped to UCLA are bin 7 only
2 bins for each type gives ±2 ns (okay)
Eventually can calibrate every chip with beam
External board handles up to 672 channels:
- All I/O
- FIFOs for dynamic test
- Delay chips for 0.25ns adjustment

Boards being debugged and firmware under development:
- ALCT-TMB test works at 40 MHz
- AFEB-ALCT test works for 16 channels at a time at 10 MHz, currently
- Nice software environment developed
Mezzanine Cards and FPGAs

- 70 bare mezzanine cards produced (also used for TMB, MPC)
- Gold immersion surface treatment much better than previous (flatter)
- 100 Xilinx XCV600E-7FG680C received, also Eproms and other parts
- Should ship next week to assembler
First TMB prototype recently produced (2 available)

VME readout now working

ALCT-TMB interface including 80 MHz data transfer from/to ALCT has been verified
ALCT-TMB Testing

- Using DYNATEM to communicate from a Linux PC to the VME crate.
- New software has been written to control TMB functions using socket connections.
- Combined test of ALCT and TMB.
- Injected patterns into the delay lines of the ALCT using self triggering.
- Looked at the results on TMB side.
- Firmware decodes the multiplexed data coming from the TMB
- Each bit checked at TMB and again through VME at DMB.
- Currently some problem getting DDU readout synchronization
TMB Current Status

• 2 TMBs were received about Nov 20, assembly of others was purposely delayed until basic debugging
• I/O of first boards checked by Dec 10, other functions by Dec 18 -> okay for assembly
• 9 boards due today, 7 next Tuesday (~4 weeks to debug)
• Suggested change for external triggering to L1A generation change for CCB firmware, Mike implemented.
• Lots of problems with PHOS4 programmable delay chips
  • Don’t power up in clocking state (dead board!)
  • Very asymmetric (58/42%) output clock
  • 5ns delay sometimes becomes 10ns etc.
• ALCT-TMB-DMB readout thru VME has been demonstrated at UCLA…
  • But not yet all the way to DDU
  • Problems with synchronization
## TMB Status

- **Synchronization problem (example):**

<table>
<thead>
<tr>
<th>Delay (ns)</th>
<th>ALCT→TMB</th>
<th>TMB→ALCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>1</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>2</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>3</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>4</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>5</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>6</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>7</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>8</td>
<td>OK</td>
<td>Bad</td>
</tr>
<tr>
<td>9</td>
<td>Errors</td>
<td>Bad</td>
</tr>
<tr>
<td>10</td>
<td>Bad</td>
<td>Bad</td>
</tr>
<tr>
<td>11</td>
<td>Bad</td>
<td>Bad</td>
</tr>
<tr>
<td>12</td>
<td>Bad</td>
<td>Bad</td>
</tr>
<tr>
<td>13</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>14</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>15</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>16</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>17</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>18</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>19</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>20</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>21</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>22</td>
<td>Bad</td>
<td>OK</td>
</tr>
<tr>
<td>23</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>24</td>
<td>OK</td>
<td>OK</td>
</tr>
</tbody>
</table>
Preliminary layout of both boards done
ALCT-672 ch version now finalized, PC board quotes received from 1 vendor:

- Per board cost is okay, but high setup fee ($3K) due to large board
Test Pulse Cables

- Have ordered 17000 ft of non-halogen cables – delivery Feb 10.
- Have ordered crimp tool (delivery Jan 24)
- Will order (next week) 5000 lemo connectors
  - Delivery as long as 4 months + 1000 connectors/month
ALCT Tracking Database

- Set up by Igor Vorobiev at CERN according to our desire
- Web viewing
- Web updating
- Works great!
Use of CLCT Information in ME1a Trigger

On-chamber electronics

Peripheral Crate electronics

ALCT

CFEB

CFEB

CFEB

CFEB

DAQ

DMB

LCT*L1A

TMB

Trigger

On-chamber electronics

Peripheral Crate electronics
Cathode (CLCT) Trigger Patterns Used

- Half-strip units for high-Pt trigger
- Simultaneously, di-strip units for low-Pt trigger
- 7 patterns of each type (fix middle at 4th layer):

1 (straight)  2 (top-)  4 (bottom-)  6 (steep-)

3 (bottom+)  5 (top+)  7 (steep+)

(3, 5, 7 are Mirror reflections of 2, 4, 6)
Minimum Bias CLCT Patterns

- Minimum Bias data sample:
  - More di-strip patterns than half-strip
  - Small number (8.5%) of nearly-straight CLCTs
  - Note that distrip CLCT about 4x the half-strip CLCT rate

- High-Pt (>10 GeV/c) muon sample:
  - 97% in central peak
DMB (DAQ MotherBoard) Readout Scheme

- CSC cathode readout is initiated by time coincidence of local trigger signal (LCT) and Level 1 accept (L1A)
- Presently use CLCT*L1A coincidence
- Could use ALCT*L1A but rates may be high
- ORCA simulation shows:
  - ALCT rate in ME1/a is 180 kHz per chamber
  - If L1 rate is 75 kHz and time coincidence window 100ns, then ALCT*L1A minimum (no correlations) DAQ rate is 1.34 kHz/chamber
  - At 3 kB per LCT, ALCT*L1A gives 300 Mbyte/sec data volume (50% of all CSC)
- New result:
  - High-momentum muons populate only straightest cathode trigger patterns
  - Cutting on cathode pattern eliminates most low-momentum backgrounds
  - Reduces DAQ volume by 12x
  - Recommend to allow CLCT*L1A readout in ME1/a
ME1 Sectors

- One peripheral crate per sector
- All ME1 chambers subtend 10°
- New scheme requires 30° sectors
- Nice feature: extra CFEB connects to empty spigots on peripheral electronics
- Re-scope will be difficult because it requires 20° sectors, hence:
  - More crates
  - More cards
  - Re-cabling
  - New daisy chain for ALCT signals
  - New ME1 backplane

<table>
<thead>
<tr>
<th>Previous ME1/a</th>
<th>Descoped ME1/a</th>
</tr>
</thead>
<tbody>
<tr>
<td>20° sectors</td>
<td>30° sectors</td>
</tr>
<tr>
<td>2 x ME1/3</td>
<td>3 x ME1/3</td>
</tr>
<tr>
<td>2 x ME1/2</td>
<td>3 x ME1/2</td>
</tr>
<tr>
<td>2 x ME1/1</td>
<td>3 x (ME1/1+ME1/a)</td>
</tr>
<tr>
<td>2 x ME1/a</td>
<td></td>
</tr>
</tbody>
</table>

VME Crate Slots

<table>
<thead>
<tr>
<th>Previous ME1/a</th>
<th>Descoped ME1/a</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 x DMB</td>
<td>9 x DMB</td>
</tr>
<tr>
<td>8 x TMB</td>
<td>9 x TMB</td>
</tr>
<tr>
<td>1 CCB</td>
<td>1 CCB (clocking)</td>
</tr>
<tr>
<td>1 MPC</td>
<td>1 MPC (trigger out)</td>
</tr>
<tr>
<td>1 VME controller</td>
<td>1 VME controller</td>
</tr>
<tr>
<td>19 cards total</td>
<td>21 cards total - FULL</td>
</tr>
</tbody>
</table>