ALCT Production Plans

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- ALCT2000 experience
- ALCT2001 improvements needed
- Pre-production status
- Production plans
ALCT2000 Experience

6 boards were produced April 2000
BGAs on large boards are problematic
  • Connections would break when board flexed
Performance was good
Altera radiation performance marginal
Not all details worked out (radiation resets, self-testing)
Changes from ALCT2000 to ALCT2001

- Altera (AHDL) changed to Xilinx (Verilog)
- FPGA placed on small mezzanine card, high-density connectors to main board
- Stiffener plate for mezzanine card
- Delay ASICs added pattern register for testing
- Added 40->80 MHz bus multiplexors to solve signal I/O to FPGA problem
- Add protocol for hard reset from TMB
- Unipolar power for pulse generator
- Added JTAG chain multiplexing – 4 independent JTAG chains on ALCT
ALCT2001 Experience

• 6 base boards were produced August 2001
• 14 mezzanine boards have been produced
• Bench and cosmic ray (+source) performance is good
• Cosmic ray testing continues
• Did 2 radiation tests ($1^{st}$ w/XCV1000E, $2^{nd}$ w/XCV600E)
• Radiation resistance: ~1/5 the SEU rate plus 4x faster reloading -> 20x less deadtime for CMS reloading.
• Reliability is good but not perfect
  • Need to work with assembler to reduce solder errors (typically 6 per base board, <1 per mezzanine board)
  • Some BGA connections lost: treatment of mezzanine card (e.g. gold immersion or white tin methods) should help
• Only modest technical improvements are needed
Changes from ALCT2001 to ALCT2001b

Mechanical:

• Add bolts to hold mezzanine card to ALCT base card.
• Move jumpers and test points out from underneath mezz card, move vias out from under mezz stiffener plate.

Electrical:

• Rad-tolerant regulator.
• Fix power-on latch-up problem.
• Reduce number of buffers used in clock distribution (minimize skew).
• More precise thresholds and power voltage readings (ADCs and DACs).
• Change values of capacitors on mezzanine card for optimum high-frequency filtering.
• Add place for power-up holdoff chip for when used without TMB hard reset control (e.g. for Muon Port Card).
• Fix board ID chip layout.
• Add some test points, add clear labels, change power LEDs from green to red (so 1.8v LED will light up).
• All modifications have been made and carefully checked on schematics and layout
• Batch of 30 bare boards received
• Batch of 70 mezzanine cards in production (also used for TMB, MPC)
• Assembly is waiting for some parts to arrive (P.O.’s have been placed)
• Boards will be tested with production test board
• Acceptable quotes were received for all production-quantity PCB manufacture and assembly, same firms
ALCT Production Testing

- Single-cable testing finds I/O problems
  - Find ~6 errors (e.g., solder bridges) per prototype board, working with assembly company
- External board handles up to 672 channels:
  - All I/O
  - FIFOs for dynamic test
  - Delay chips for 0.25ns adjustment
- Boards being debugged and firmware under development
ALCT-672 and –288 Versions

Numbers:
- 216 ALCT-384, 144 ALCT-288 (if ME1/1), 108 ALCT-672 (if ME4/1)
- Add 10% working spares

Preliminary layout of both boards done
ALCT-672 ch version finalized ~1 week
Delay ASICs

Produced and tested by Carnegie-Mellon
Chips in production testing phase
Delay slope varies substantially
At code=15 (max delay), data bins:

1. 42 ns - 25 chips  1.6 ns/div  "road" = 3.3 ns
2. 44 ns - 85 chips  1.7 ns/div  "road" = 4.8 ns
3. 46 ns - 150 chips 1.8 ns/div  "road" = 4.3 ns
4. 48 ns - 185 chips 1.9 ns/div  "road" = 4.5 ns
5. 50 ns - 290 chips 2.0 ns/div  "road" = 4.8 ns
6. 52 ns - 330 chips 2.1 ns/div  "road" = 4.7 ns
7. 54 ns - 586 chips 2.2 ns/div  "road" = 4.7 ns
8. 56 ns - 373 chips 2.3 ns/div  "road" = 4.5 ns
9. 58 ns - 99 chips  2.4 ns/div  "road" = 4.3 ns

Use “bins” 3-8 only (45-57 ns)
Actual slope set by external resistor
Different resistor choices for ALCT-384/672/288 to equalize somewhat
First Delay ASICs shipped to UCLA are bin 7 only
2 bins for each type gives ±2 ns (okay)
Eventually can calibrate every chip with beam
FPGAs

• First 6 mezz: Xilinx XCV1000E-7FG680
  • Cost ~$1000
• Next 8 mezz: XCV600E-7FG680
  • cost ~$600
• Target for ALCT-384 and –288 is the XCV600E
  • Design uses 75% of logic cells
  • Plenty of routing resources
  • Maximum speed is 45 MHz (conservative)
• For ALCT-672, must use XCV1000E
• (For Trigger Motherboard and Muon Port Card mezz cards, can use XCV1600E, 2000E in same package)
• Cost is acceptable for ALCT budget.
• ALCT can be read out through JTAG, but slowly
• Full capability requires TMB clocking and readout
• 18 TMB boards have been produced for all CSC test sites, including spares
• 2 boards have been delivered and are being debugged, 16 will be assembled ~3 weeks
• VME registers and ALCT interface debugged
• Plan to ship to FAST sites for system debugging ASAP (few weeks)
Production Plans

- Schedule set by installation schedule, working backwards:
  - YE2 chambers installed at CERN starting in fall ’02
  - Chambers received and simple tests at CERN summer ’02
  - Chambers tested at FAST sites in spring ’02
  - FAST sites need to debug testing of chambers with full set of electronics (CFEB, AFEB, ALCT, DMB, TMB, CCB) starting as soon as possible
  - Chambers are stacking up at FAST sites waiting for electronics and checkout
- Hard-to-get parts already ordered (Oct 2000 ESR)
- Debug first 30 pre-production boards
- Deliver first 10 boards ASAP (late Dec) for use at FAST sites
- Order full quantities of most parts (20% spare boards/parts, 30% spare ASICs)
- Deliver 20 boards ~February
- Deliver 7 prototype ALCT-672 ~February
- Order 200 ALCT-384 PCBs in spring 2002
- Pace of electronics delivery set by testing schedule, but should easily exceed chamber production rate, catch up ~April 2002
Possibility of Virtex-II on mezzanine card:
- Allows better capacity/cost, and higher maximum capacity
- Different (better?) SEU characteristics
- Requires ~2 months additional engineering to do layout
- Higher speed is attractive for final TMB (e.g. ~50 -> ~80 MHz)
- Drawbacks:
  - no flexibility in chip selection (E-series layout handles 600E through 2000E chips).
  - Requires 1.5v core voltage (different LVDB resistor choice)
  - Very high density: for instance, where to put power filter capacitors?
- Can save on FPGA costs (~500 units TMB, maybe ~500 ALCT):

<table>
<thead>
<tr>
<th>Virtex-E chip</th>
<th>Price</th>
<th>Virtex-2 equivalent</th>
<th>Price</th>
<th>Savings @500 units</th>
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<tbody>
<tr>
<td>XCV600E-7FG680C</td>
<td>$600</td>
<td>XC2V1000-5FF896CES</td>
<td>&lt;$532</td>
<td>&gt;$34K</td>
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<td>XCV1000E-7FG680C</td>
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<td>(XC2V3000-4BG728CES)</td>
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<td>XC2V3000-4BG728CES</td>
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</table>
Conclusions

• CSC installation schedule requires timely approval for production
  ALCT2001 meets CMS requirements
• Board is well-engineered for production
• Pre-production batch is being assembled
• Approval for production?