ALCT Production, Cable Tests, and TMB Status

- ALCT production status
  - Production schedule
  - Required board modifications
  - Pre-production batch
  - Production testing progress

- Cable test results
  - Tyco (2 variants) versus Skewclear

- TMB status
  - Board production
  - Firmware

- Status of ALCT 672- and 288-ch variants

- AOB
Near-term ALCT Schedule

✓ Sept: Finish debugging of first 6 boards and self-test firmware
✓ Sept. 26: first radiation test
  • October: Finish radiation tests and validation
  • ~Dec 1: Production approval at ESR
  • Agreement with Korytov:
    • Nov. 20: Batch of 10 ALCT-384 shipped (2+ TMBs required).
    • Jan. 2, 2002: Batch of 20 ALCT-384 shipped
    • Jan. 7, 2002: Batch of 7 ALCT-672 shipped

• Validation used to appear to be the major bottleneck, now concentrating on production-related issues.
• In 2002, production/testing rate is not a problem (catch up with chamber production/testing rapidly)
New ALCT Boards

- Power, computer connectors
- 80 MHz SCSI outputs (to Trigger Motherboard)
- Analog section:
  - test pulse generator,
  - AFEB power,
  - ADCs, DACs
- Input signal connectors
- Xilinx mezzanine card
- Delay/ buffer ASICs, 2:1 bus multiplexers (other side)
- Main board for 384-ch type

Analog section:
- test pulse generator,
- AFEB power,
- ADCs, DACs (other side)
Summary ALCT Status

- **Hardware:**
  - Prototype batch of 6 ALCT2001-384 boards produced
  - 15 Mezzanine cards produced, 6 of these assembled.
  - Debugging of these boards is ongoing:
    - Slow Control functions are now fully debugged.
    - Virtex (trigger, readout) functions mostly debugged.
  - Variants: first version of ALCT-672 is complete, ALCT-288 is ongoing
  - Some design changes will be made
  - Order placed for production test boards, assembly to follow

- **Firmware/software:**
  - Self-test firmware and software available for Slow Control and Virtex.
  - Downloading from Linux under development
  - Missing pieces: front-end AFEB bits readout, integration with TMB.
ALCT Modifications Required

Mechanical:
• Add bolts to hold mezzanine card to ALCT base card.
• Move jumpers and some test points out from underneath mezz card.

Electrical:
• Adopt known rad-tolerant regulator for test pulse circuit.
• Change reference voltage from 2.5v to 1.225v for better threshold control.
• Change ADC chip from 8 bits to 10 bits (pin-compatible).
• Modify test pulse circuit to get maximum amplitude 1.0v at DAC=255.
• Change small capacitors on mezzanine card for better high-frequency filtering.
• Add some test points, add clear labels.
• Change LEDs from green to red (so light up at 1.8v).
• Concern about power-on latchup under some circumstances (AM).

Firmware:
• Add input data FIFO and readout, hot channel mask, etc. to Virtex chip.
• Add shadow registers to Virtex chip to allow readback of settings.
ALCT Production Testing

- Full test requires external connections:
  - FPGA loaded from PC // port
  - Testing program loads FIFOs on test board
  - Test board outputs driven at 40 MHz, Virtex FPGA looks at inputs
  - Two data paths to test:
    - Input side AFEB-ALCT path
    - Output side ALCT-TMB path
  - Fine timing tested with delay curves (0.25ns setting accuracy)
- Board being manufactured (arrive Oct. 15)
- Firmware under development
ALCT-TMB Cables
(80 MHz + Clocking signals)

- Automatic cable-tester not adequate for cable selection (go-nogo)
- Skew, attenuation, cross-talk examined by hand
- 2 cables from Tyco tested
  - Madison cable: Skew ~1.5ns, risetime ~1ns
  - Sumitomo cable: Skew ~1.3ns, risetime 2-2.5ns, large attenu.
- 1 Skewclear cable tested
  - Skew <0.5ns, risetime ~1 ns. Known to work up to 280 MHz. Clearly the best quality cable.
- Madison cable from Tyco would probably work at 80 MHz, about $240/cable/12 meters.
- Rumored $240/cable cost for 30-gauge Skewclear – clear choice.
- Should OSU handle procurement for combined order? Cable testing?
• VME 9U card with interfaces to
  • ALCT (input)
  • 5xCFEB (input)
  • DMB (DAQ output)
  • CCB (clocking)
  • MPC (trigger output)
  • RPC link boards (optional, input)
• 22 boards have been produced.
• 2 boards will be delivered Oct 2020.
• 18 assembled following approval.
Trigger Motherboard Firmware

- Firmware adapted from previous CLCT99 and TMB99
- Altera+AHDL to Xilinx+Verilog conversion
- Up to speed on Xilinx/Verilog learning curve
- Clocking and fine adjustments (DLL) done
- CLCT code half done (so far 1 clock faster)
- VME section (central) almost done
- ALCT pass-thru still to do
- TMB coincidence still to do
Preliminary layout by M. Kan (PNPI)
Updates will follow lead of ALCT-384
First boards (7) of ALCT-672 will be ordered late-November
Pre-production Plan

• ~Dec 1: Production approval at ESR

• Agreement with Korytov:
  • Nov. 21: Batch of 10 ALCT-384 shipped
  • Jan. 2: Batch of 20 ALCT-384 shipped
  • Jan. 7: Batch of 7 ALCT-672 shipped
  • Jan 18: Batch of 12 ALCT-384 shipped
  • Feb 18: Batch of 10 ALCT-384 shipped
  • Etc.

• Boards required before CERN ESR
• Minor changes now being implemented

• ALCT-384:
  • Next step place order for 46 PC boards by Oct 10, assemble 10 by Nov. 2 etc.
  • Testing/debugging at rate of ½-2/3 board/day initially

• ALCT-672:
  • place order for 8 PC boards by Oct. 22 allows to meet schedule
• 2 prototype ALCTs -> FAST sites about October 20 (with JTAG readout)?
• Possibility of Virtex-II on mezzanine card:
  • Allows better capacity/cost, and higher maximum capacity
  • Different (better?) SEU characteristics
  • Requires ~2 months additional engineering to do layout
  • Higher speed is attractive for final TMB (e.g. ~50 -> ~80 MHz)
  • Drawbacks:
    • no flexibility in chip selection (E-series layout handles 600E through 2000E chips).
    • Requires 1.5v core voltage (different LVDB resistor choice)
    • Very high density: for instance, where to put power filter capacitors?
  • Can save on FPGA costs (~500 units TMB, maybe ~500 ALCT):

<table>
<thead>
<tr>
<th>Virtex-E chip</th>
<th>Price</th>
<th>Virtex-2 equivalent</th>
<th>Price</th>
<th>Savings @500 units</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCV600E-7FG680C</td>
<td>$600</td>
<td>XC2V1000-5FF896CES</td>
<td>&lt;$532</td>
<td>&gt;$34K</td>
</tr>
<tr>
<td>XCV1000E-7FG680C</td>
<td>$1193</td>
<td>(XC2V3000-4BG728CES)</td>
<td>(&lt;$1142)</td>
<td>&gt;$25K</td>
</tr>
<tr>
<td>XCV1600E-7FG680C</td>
<td>$1843</td>
<td>XC2V3000-4BG728CES</td>
<td>&lt;$1142</td>
<td>&gt;$350K</td>
</tr>
<tr>
<td>XCV2000E-7FG680C</td>
<td>$2865</td>
<td>XC2V3000-4BG728CES</td>
<td>&lt;$1142</td>
<td>&gt;$862K</td>
</tr>
</tbody>
</table>