CSC Endcap Muon Trigger

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Talk Outline

• Brief introduction to CSC trigger system
• On-chamber electronics status report
• Off-chamber electronics status report
• Future plans and schedule
CMS Endcap Muon System

- 3 or 4 stations
- Each CSC chamber has six planes:
  1. Radial cathode strips for precision muon position and bend direction measurement
  2. Anode wires for timing (bunch ID) and non-bend position measurement
CSC Muon Triggering

- Goal: send only the highest quality muon tracks to Global L1
- Trigger primitives are wire and strip segments
  - Wires give 25ns bunch crossing
  - Strips give precision $\phi$ position information
- Link trigger primitives into tracks
- Assign $p_T$, $\phi$, and $\eta$
CSC Endcap Muon Trigger Responsibilities

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USCMS Endcap Muon

OSU 1.2.1

Cathode Front-End

CFE

Anode Front-End

CMU 1.2.2

Anode LCT

RPC in.

Cathode LCT/Motherboard/RPC

LCT

TMB

MPC

Port Card

OPTICAL

Sector Receiver

SR

SP

Sector Processor

CSC Muon Sorter

Global Trigger

Global L1

Vienna

Also: 3.1.1.7 Backplanes - Florida
3.1.1.8-11 controllers, crates, power supplies, cables

Clock & Control1

Rice

Clock & Control2

Rice

Also: 3.1.1.5

USCMS Trigger/DAQ 3.1.1

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USCMS Trigger/DAQ 3.1.1
Locations of CSC Trigger Electronics

Endcap Muon:
- Comparator ASICs, ALCT card
- CLCT/Motherboard, Port Cards

(Tridas: Sector Receiver, Sector Processor, Muon Sorter, Clock&Control Cards)

Peripheral Electronics
- Optical Fiber ~100m
- Muon Stubs (LCT) Found, DAQ readout
- Counting House Electronics
- Muon Tracks Found

On-Chamber Electronics
- On-chamber Electronics
- Copper (Channel Links) ~8m

Peripheral Crates
- 9U CRATES
- Anode Trigger “LCT” Board
- Cathode Front-End Boards
- Anode Front-End Boards

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Previous Prototypes

- 1997: very first prototype “proof of concept”
- 1998: focus on trigger primitive performance
- 1999: focus on trigger primitive engineering
- 2000: built and tested lower-cost ALCT-384, also built and tested Track Finder (TRIDAS) components
1) Comparator ASICs

- Compare pulse heights from adjacent strips to find position of muon to ½-strip
- Design finalized (JC Santiard, CERN)
- Mounted on CFEB boards
- Production of 48 wafers (35K chips) is proceeding
- Pre-production yields 60-70%, lower than expected
- Testing:
  - 1500 done by hand, 2500 more needed (June)
  - Automated testing: trouble with commercial firm
  - Semi-automatic procedure under development (Sept.)
2) ALCT “Anode Local Charged Track”
   • Use anode hits to find track and 25ns bunch crossing
   • 2000 prototype worked well but radiation-soft FPGAs
   • Redesigned in Xilinx technology
   • High-density 288, 384, and 672-channel versions reqd.
   • Redesign nearly complete
     • FPGA mounted on mezzanine board, layout done
     • Motherboard schematics done, routing 90% done
   • Production slated to start in summer
     • Slipped some weeks due to PNPI engineer changes
     • Test facility under development
     • Test board fully routed
     • Test firmware under development
• Delay/translator ASIC on input
• Three types of FPGA:
  • 4-7 LCT chips handle 96+ wire inputs
  • One Concentrator prioritizes stubs, central logic (state machines)
  • One Slow Control chip interfaces to analog functions
• ADCs, DACs, test pulse generator
• Output Clinks
ALCT Conversion to Xilinx

The situation:

- Spring 2000: ALCT prototype built
- Summer: radiation tests
  - Altera FPGAs upset ~daily/chip at LHC
  - need re-booting from flash RAMs
- November: Management decision
  - convert firmware and technology to Xilinx, which reloads much faster
- ALCT is on Emu critical path
- Conversion requires time and additional resources

The response:

- Added engineering (PNPI) to recover schedule
New ALCT Layout

Previous version:
- Channel-Links to SCSI output connectors
- Concentrator FPGA
- 96-ch ALCT FPGAs
- Delay/ buffer ASICs
- Input connectors
- Analog section: Pulser, AFEB power and control

New version:
- Xilinx mezzanine card
- Motherboard
ALCT2001 Modifications

- Change from Altera AHDL to Xilinx (Verilog) XCV600E, 1000E, or 1600E (identical packages)
- Replace multiple BGAs by single chip on mezzanine card
- 40-to-80 MHz multiplexors required
- Hard reset signal from TMB starts reload of FPGAs from EEPROMs
- Delay chips allow pattern loading, test of BGA input ball connections
- All signals on 2 SCSI-50 connectors
- Implement 4-way JTAG multiplexor
ALCT Production Testing

- Boards tested before and after baking in oven at FNAL
- Internal tests from delay chips to output of trigger FPGA
- Full external connection tests:
  - FPGA loaded by JTAG
  - Special testing program drives outputs and looks at inputs
  - Two paths:
    - Input side AFEB-ALCT path
    - Output side ALCT-TMB path
  - Pulsed testing (25ns) anticipated
Off-chamber Electronics Status

• TMB “Trigger Motherboard”
  • Combines functions of previous CLCT and TMB boards, adds RPC link interface
  • CLCT finds track positions from half-strip bits
  • TMB correlates anode and cathode views by timing
  • DAQ path for anode and trigger bits through DMB
  • RPC interface can resolve CSC muon ghosts

• Schedule
  • Prototype under development, needed for ALCT and CFEB comparator readout
  • Schematics nearly done
  • Layout will be done by commercial firm
Previous CLCT99 & TMB99

480 input strips
Find 4-6 layer patterns
Raw hits in DAQ FIFO

Strips/wire coincidence, readout FIFO
TMB2001 Structure

- Uses same Xilinx mezz. card as ALCT
- 30-page spec. document
- I/O count 452
  - 313 inputs
  - 7 clocks
  - 146 outputs
- Schematic capture nearly complete
Schedules

• On-chamber electronics schedule is driven by FAST site testing. Off-chamber electronics schedule is more relaxed.

• On-chamber comparator ASICs
  • Production testing needs to be sorted out (but enough time)

• On-chamber ALCT boards
  • First prototype ready for test in ~4 weeks
  • Production testing apparatus ready in ~6-8 weeks
  • First production batches this summer
  • 672 and 288-channel versions follow 2, 4 months later (limited by PNPI layout engineering). Schematics already underway.

• Off-chamber TMB boards
  • 6 boards will be produced this summer
  • Pre-production prototype next year will implement all fixes found during testing
  • Production starts in mid-2002
Personnel

• Professors
  • Jay Hauser (UCLA), Paul Padley (Rice)

• Postdocs
  • Benn Tannenbaum (UCLA), Martin von der Mey (UCLA)

• Engineers
  • JK (UCLA), Alex Madorsky (Florida), Mike Matveev (Rice), Jean-Claude Santiard (CERN)

• Guest engineers (all PNPI)
  • Valeri Iatsioura, Misha Kan, Gennady Zhmakin
Responsibilities

Comparator testing
  Santiard (CERN) and Von der Mey (UCLA)

ALCT2001-384 schematics and layout
  Sedov (departed) and Iatsioura (PNPI, at UCLA)

Xilinx mezzanine card schematics and layout
  Iatsioura

“Xblaster” parallel-to-JTAG LVDS
  Kan (PNPI) and Shi (UCLA)

Schematics and layout for ALCT 672ch and 288ch variants
  Kan

Production supervision of ALCTs
  Iatsioura

Production testing of ALCT and later TMB
  Zhmakin (PNPI, at FNAL) and Lindgren

Radiation tests
  Von der Mey

TMB schematics, firmware, prototype testing
  JK (UCLA)

TMB layout and assembly
  Subcontracted to industry
FY 2000 focus was on producing and testing a Track Finder prototype during summer:

Results included in Trigger TDR (Oct. 2000):

- Input data bits loaded into Port Card or SR
- Data clocked through MPC SR SP at full speed
- Results examined for validity
Conclusions

Concerns:

• The CSC muon tracks must reach the Global Muon Trigger <1975 ns after the crossing. The current electronics are about 30% too slow, but new FPGAs and one-chip TMB and SP solutions should allow this.

• Verilog language firmware support for ALCT – developed by Razmyslovitch (departed for industry), ultimately would like physicist control.

• By 2004 (end of Project), engineering support will largely go away.

Base program cutbacks will definitely hurt this project

• CSC trigger requires careful optimization simulation studies by physicists

• Almost all VME control software is developed by physicists

• Post-docs and students should control the trigger “knobs” that are in FPGAs

• UCLA has 1.0 FTE postdoc on this project, Rice has 0.0 FTE postdocs.

• Additional postdoc simulation support from other programs at UC Davis-Ko (1.0 FTE postdoc), UCLA-Cousins (0.5 FTE) and Caltech-Newman (0.3 FTE postdoc)