Comparator and ALCT Status Report

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@ Comparator pre-production status
@ Comparator radiation tests
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@ ALCT2000 radiation tests
@ AOB
Comparador ASICs on Cathode FEB

**Versions:**

1997
- Low noise
- Output data compression

1998
- Comparator ASICs on Cathode FEB

1999
- Comparator ASICs

**Functionality:**

- Q_strip
- Output data compression
- Half-strip bit
- Coded "triad" bits
- Strip
- Di-strip
- Half-strip

**Results:**

- Perfect resolution $\sigma=0.29$ half-strip
- No source: $\sigma=0.36$ half-strips
- CMS max rate: $\sigma=0.38$ half-strips

Emu meeting at CERN, June 2000
Comparator ASIC Status

• Two pre-production wafers received from IMEC, sent for packaging:
  • 540 chips to test
  • about 420 useable chips anticipated

• Testing planned for CERN chip tester:
  • Labview program for testing is being developed by Adance firm
  • Special test board also being built

• Chip testing will begin end of June
  • Sample yield and performance

• Full ASIC submission is possible Fall 2000 after CSC electronics Engineering System Review
Comparator ASIC
Radiation Tests

- Davis cyclotron used for radiation tests:
  - 63 MeV proton beam ionizes, simulates LHC neutron effects
  - 10 LHC years = 1.7 kRad ionizing, 300 kRad neutron

- Continuous monitoring of threshold and offset (ionizing damage)

- Continuous monitoring of power supply current (latch-up due to neutrons)

- Comparator test results:
  - May 8 exposure
  - No change in threshold/offsets up to 15 kRad exposure
  - Current rises after 15 kRad, chip stops functioning at ~50 kRad (ionization damage)
  - No latchup observed to 300 kRad

- Next test: June 5 (tomorrow) with more chips
Algorithm:

Wire group number

<table>
<thead>
<tr>
<th>n+2</th>
<th>[parallel]</th>
</tr>
</thead>
<tbody>
<tr>
<td>n+1</td>
<td>[parallel]</td>
</tr>
<tr>
<td>n</td>
<td>[parallel]</td>
</tr>
<tr>
<td>n-1</td>
<td>[parallel]</td>
</tr>
<tr>
<td>n-2</td>
<td>[parallel]</td>
</tr>
</tbody>
</table>

abc def layer

Circuit board:

- Channel-Links to SCSI output connectors
- Concentrator FPGA
- 96-ch ALCT FPGAs
- Delay/ buffer ASICs
- Input connectors
- Analog section: Pulser, AFEB power and control

Efficiency:

- ME1/a
- ME1/1
- ME1/2
- ME1/3
- ME2/1
- ME3/1
- ME2/2
- ME3/2
- ME4/1
- ME4/2

ALCT99 Efficiency
**Testing:**
- Board tests at UCLA in March
- First chamber tests at Fermilab late April
- Triggering works fine, board features work well
- Bugs: JTAG buffer needs more current drive, test pulse inverted, not enough time bins stored in FIFO for input bits readout when externally triggered...

**Board modifications for pre-production version:**
- Stiffening added
- Combine 2 SCSI + 2 JTAG connectors/cables into one connector
- Add refresh signal (single event upsets from radiation)
- Move AFEB fuses to top of board

**Next tests at Fermilab as per Dolinsky schedule in June**
ALCT2000 Radiation Tests

- **Davis cyclotron used for radiation tests, May 15:**
  - Altera LCT and Slow Control FPGAs, flash RAMs, ADCs, DACs, temp sensor
  - Continuous self-test program (single-event upset detection or ionization damage), LCT and input FIFO data written to disk
  - Continuous monitoring of power supply current (latch-up due to neutrons)

- **Preliminary test results:**
  - [http://www-collider.physics.ucla.edu/cms/trigger/proto00/alct_radiation_test.html](http://www-collider.physics.ucla.edu/cms/trigger/proto00/alct_radiation_test.html)
  - FPGAs encountered “frequent” upsets every 10-500 Rad (~daily at LHC), need re-booting from flash RAMs.
  - Flash RAMs encountered no errors
  - Ionization damage to temp sensor, DACs or ADCs at ~15 kRad
  - Ionization damage to FPGAs at ~60 kRad
  - No latchup observed up to 300 kRad

- **Next test: June 6**
  - Reboot from Flash RAM on error condition to better count SEUs
  - Irradiate delay ASICs
• Track Finder (TriDas project) has not yet been prototyped
• Building a Track Finder prototype this summer:

> Input LCT data bits loaded into Port Card or SR
> Data clocked through MPC SR SP at full speed
> Track Finder results examined for validity
  • Results will be included in Trigger TDR (Oct.)

• SR and SP layouts are done, assembled boards ~2 weeks
• Backplane done
• MPC split into mother- and daughter-cards, somewhat delayed