

RPC/ALCT Transition Module RAT2004 Design

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Table of Contents

LIST OF FIGURES	2
LIST OF TABLES.....	2
RAT2004 OVERVIEW	3
RAT2004 LOGIC	4
ALCT.....	4
RPC.....	4
LEDs.....	4
RAT2004 CONNECTORS	5
RAT Connector Summary	5
J1-J4 RPC0-RPC3 Connectors	6
J5 ALCT Cable A Connector (Receiver).....	7
J6 ALCT Cable B Connector (Transmitter).....	8
J5-J6 SCSI-II 50-Pin Connector Pin Convention.....	9
ALCT Cable Connections.....	10
P3B Backplane RPC+ALCT Connector	11
PCB Shunts.....	12
REVISION HISTORY.....	13

List of Figures

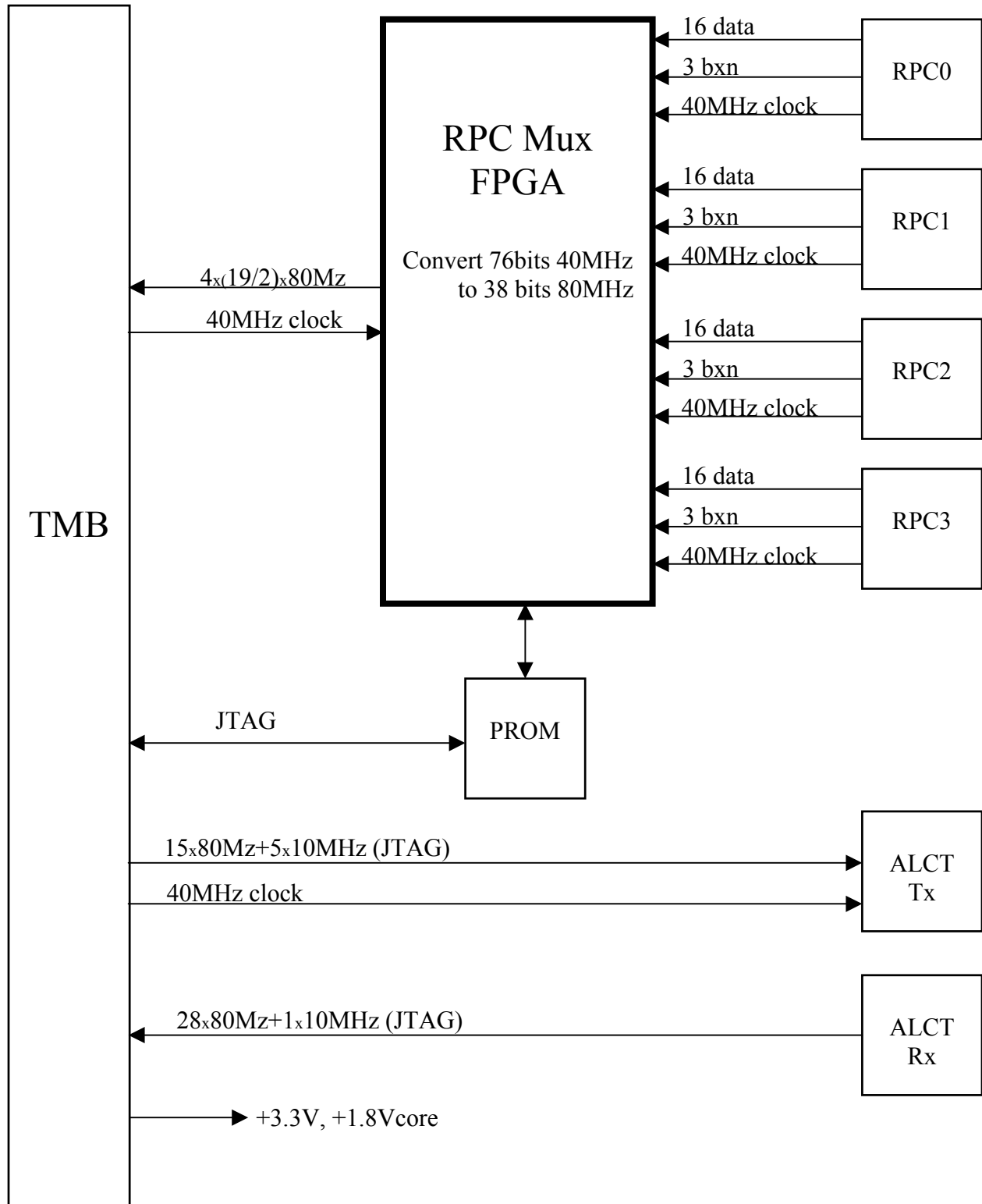
Figure 1: RAT2004 Overview	3
Figure 2: 50-Pin PCB Connector (Female)	9
Figure 3: 50 Pin Cable Connector (Male).....	9
Figure 4: 50 Pin PCB Connector Pin Convention	9

List of Tables

Table 1: RAT Front Panel LEDs	4
Table 2: RAT2004 Connector Summary	5
Table 3: J0-J4 RPC-to-RAT Connectors	6
Table 4: J5 ALCT Cable A Connector [J10 on ALCT board]	7
Table 5: J6 ALCT Cable2 Connector [J11 on ALCT board]	8
Table 6: P3B Backplane RPC+ALCT Connector	11

RAT2004 Overview

Figure 1: RAT2004 Overview



RAT2004 Logic

ALCT

The ALCT section passes 80MHz LVDS data between the Anode LCT board and the Trigger Mother Board (TMB2004). RAT2004 converts TMBs LVTTTL signals to LVDS for transmission to ALCT, and converts ALCT signals from LVDS to LVTTTL. It does not modify the content of the data streams.

The logic operates in two modes:

- Normal mode: Transmits 21 LVDS bits to ALCT, receives 29 bits from ALCT.
- Loopback mode: Transmits 25 LVDS bits, receives 25 LVDS bits for TMB self-test.

RPC

The RPC section receives 40 MHz LVDS data from RPC Link Boards, and multiplexes it to 80MHz for transmission to the TMB. This is done to conserve TMB FPGA I/O pins.

RAT2004 receives RPC data[15:0], a bunch-crossing-number BXN[2:0], and a 40MHz clock from up to 4 RPC Link Boards. Shunts SHN[4:1] and SHP[4:1] allow optionally grounding the signal BXN[2] to provide a ground reference for the LVDS receivers.

The 80MHz multiplexing function is performed in a Xilinx XC2S50E FPGA.

A JTAG-programmable EPROM loads the FPGA on power-up or when TMB issues a hard reset signal to RAT2004. TMB provides JTAG signals to RAT from VME or an X-Blaster.

Multiplexer logic in the FPGA latches RPC data on either edge of the 40 MHz RPC clock (selected by the TMB rpc_posneg signal), and can implement DLL-adjustable clock delays if needed.

The RPC data processing sequence is:

- 1) Latch RPC data
- 2) Synchronize to TMBs 40MHz clock
- 3) Multiplex outputs 2-to-1 at 80MHz

Data transmission to TMB is synchronized with TMBs local 40MHz clock by the programmable 3D3444 delay IC. Setting rpc_sync=1 puts the RAT FPGA into a synchronization mode where the 80MHz RPC output signals are set to 0 for the first 12.5ns transmission phase, and to 1 for the second phase.

LEDs

Table 1: RAT Front Panel LEDs

LED	Color	Function
0	Green	RPC 0 Clock detected
1	Green	RPC 1 Clock detected
2	Green	RPC 2 Clock detected
3	Green	RPC 3 Clock detected
4	Green	ALCT Tx Cable detected
5	Green	ALCT Rx Cable detected
6	Red	ALCT Cable Error
7	Red	RPC Cable Error

RAT2004 Connectors

RAT Connector Summary

Table 2: RAT2004 Connector Summary

ID	Pins	Type	Function
J1	40	Ribbon Header	RPC0 data + Clock + BXN
J2	40	Ribbon Header	RPC1 data + Clock + BXN
J3	40	Ribbon Header	RPC2 data + Clock + BXN
J4	40	Ribbon Header	RPC3 data + Clock + BXN
J5	50	SCSI-II	ALCT Cable A Rx
J6	50	SCSI-II	ALCT Cable B Tx
P2A	125	Z-Pack 25x5	CCB + DMB (RAT only uses GNDs)
P2B	55	Z-Pack 11x5	DMB (RAT only uses GNDs)
P3A	55	Z-Pack 11x5	MPC (RAT only uses GNDs)
P3B	125	Z-Pack 25x5	RPC to TMB+ ALCT I/O + Power

J1-J4 RPC0-RPC3 Connectors

Function: Receives 40MHz data from RPCs

Connector Type: PCB: 3M: 3432-5002
 Latches: 3M: 3505-2 (short) 3505-3 (long)
 Cable: 3M:

Table 3: J0-J4 RPC-to-RAT Connectors

Pair	Pin		Dir	Logic	Signal From RPC _n
rx0	1-	2+	In	LVDS	data[0]
rx 1	3-	4+	In	LVDS	data[1]
rx 2	5-	6+	In	LVDS	data[2]
rx 3	7-	8+	In	LVDS	data[3]
rx 4	9-	10+	In	LVDS	data[4]
rx 5	11-	12+	In	LVDS	data[5]
rx 6	13-	14+	In	LVDS	data[6]
rx 7	15-	16+	In	LVDS	data[7]
rx 8	17-	18+	In	LVDS	data[8]
rx 9	19-	20+	In	LVDS	data[9]
rx 10	21-	22+	In	LVDS	data[10]
rx 11	23-	24+	In	LVDS	data[11]
rx 12	25-	25+	In	LVDS	data[12]
rx 13	27-	28+	In	LVDS	data[13]
rx 14	29-	30+	In	LVDS	data[14]
rx 15	31-	32+	In	LVDS	data[15]
rx 16	33-	34+	In	LVDS	40 MHz clock
rx 17	35-	36+	In	LVDS	bxn[0]
rx 18	37-	38+	In	LVDS	bxn[1]
rx 19	39-	40+	In	LVDS	bxn[2]

J5 ALCT Cable A Connector (Receiver)

Function: Receives 80MHz data from ALCT.

Connector Type: PCB: AMP 787190-5
 Cable: AMP 749111-4
 Shell: AMP 749889-3 [with latches]

Table 4: J5 ALCT Cable A Connector [J10 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion = ☹

Pair	Inverted	Pin		Dir	Logic	Multiplexed Signals	
		+	-			First in Time	Second in Time
1	☹	1+	2-	In	LVDS	first_valid	second_valid
2		49+	50-	In	LVDS	first_amu	second_amu
3	☹	3+	4-	In	LVDS	first_quality0	second_quality0
4		47+	48-	In	LVDS	first_quality1	second_quality1
5	☹	5+	6-	In	LVDS	first_key0	second_key0
6		45+	46-	In	LVDS	first_key1	second_key1
7	☹	7+	8-	In	LVDS	first_key2	second_key2
8		43+	44-	In	LVDS	first_key3	second_key3
9	☹	9+	10-	In	LVDS	first_key4	second_key4
10		41+	42-	In	LVDS	first_key5	second_key5
11	☹	11+	12-	In	LVDS	first_key6	second_key6
12		39+	40-	In	LVDS	bxn0	bxn3
13	☹	13+	14-	In	LVDS	bxn1	bxn4
14		37+	38-	In	LVDS	bxn2	/wr_fifo
15	☹	15+	16-	In	LVDS	daq_data0	daq_data7
16		35+	36-	In	LVDS	daq_data1	daq_data8
17	☹	17+	18-	In	LVDS	daq_data2	daq_data9
18		33+	34-	In	LVDS	daq_data3	daq_data10
19	☹	19+	20-	In	LVDS	daq_data4	daq_data11
20		31+	32-	In	LVDS	daq_data5	daq_data12
21	☹	21+	22-	In	LVDS	daq_data6	daq_data13
22		29+	30-	In	LVDS	lct_special	first_frame
23	☹	23+	24-	In	LVDS	seq_status0	seu_status0
24		27+	28-	In	LVDS	seq_status1	seu_status1
25	☹	25+	26-	In	LVDS	ddu_special	last_frame

J6 ALCT Cable B Connector (Transmitter)

Function: Sends/Receives 80MHz data to/from ALCT.

Connector Type: PCB: AMP 787190-5
 Cable: AMP 749111-4
 Shell: AMP 749889-3 [with latches]

Table 5: J6 ALCT Cable2 Connector [J11 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion ☹

Pair	Inverted	Pin		Dir	Logic	Multiplexed Signals	
		+	-			First in Time	Second in Time
1		1+	2-	Out	LVDS	tdi	
2	☹	49+	50-	Out	LVDS	tms	
3		3+	4-	Out	LVDS	tck	
4	☹	47+	48-	Out	LVDS	jtag_select0	
5		5+	6-	Out	LVDS	jtag_select1	
6	☹	45+	46-	Out	LVDS	ccb_brcst0	ccb_brcst4
7		7+	8-	Out	LVDS	ccb_brcst1	ccb_brcst5
8	☹	43+	44-	Out	LVDS	ccb_brcst2	ccb_brcst6
9		9+	10-	Out	LVDS	ccb_brcst3	ccb_brcst7
10	☹	41+	42-	Out	LVDS	brcst_str1	subaddr_str
11		11+	12-	Out	LVDS	dout_str	bx0
12	☹	39+	40-	Out	LVDS	ext_inject	ext_trig
13		13+	14-	Out	LVDS	level1_accept	sync_adb_pulse
14	☹	37+	38-	Out	LVDS	seq_cmd0	seq_cmd2
15		15+	16-	Out	LVDS	seq_cmd1	reserved_in4
16	☹	35+	36-	Out	LVDS	reserved_in0 ¹	reserved_in2
17		17+	18-	Out	LVDS	reserved_in1	reserved_in3
18	☹	33+	34-	Out	LVDS	async_adb_pulse	
19		19+	20-	Out	LVDS	/hard_reset	
20	☹	31+	32-	Out	LVDS	clock_en	
21		21+	22-	Out	LVDS	clock	
22		29+	30-	In	LVDS	tdo	
23	☹	23+	24-	In	LVDS	reserved_out0	reserved_out2
24		27+	28-	In	LVDS	reserved_out1	reserved_out3
25	☹	25+	26-	In	LVDS	active_feb_flag	cfg_done

¹ Reserved cable input signals connect to ALCT FPGA user input pins

J5-J6 SCSI-II 50-Pin Connector Pin Convention

Figure 2: 50-Pin PCB Connector (Female)²

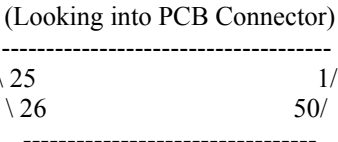


Figure 3: 50 Pin Cable Connector (Male)

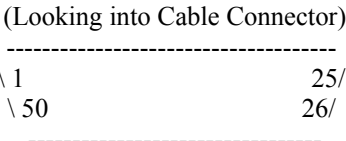
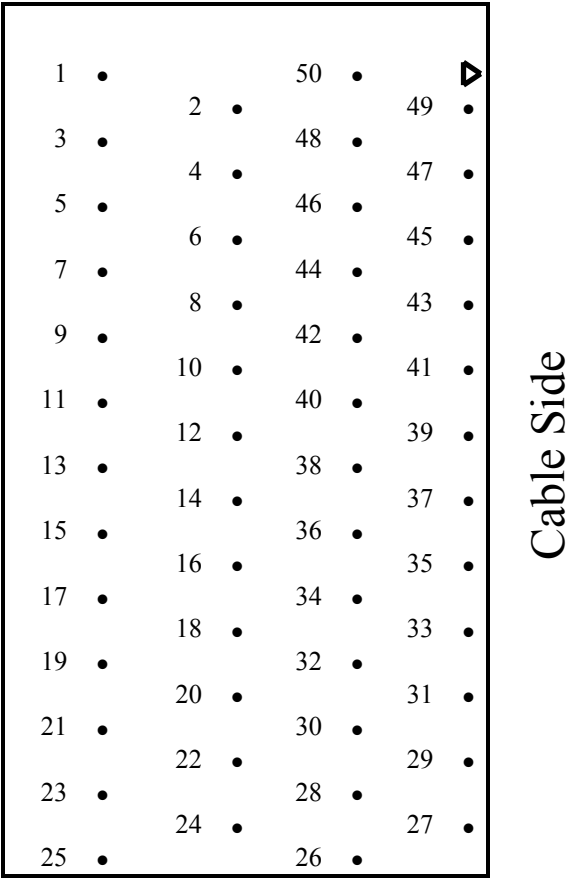


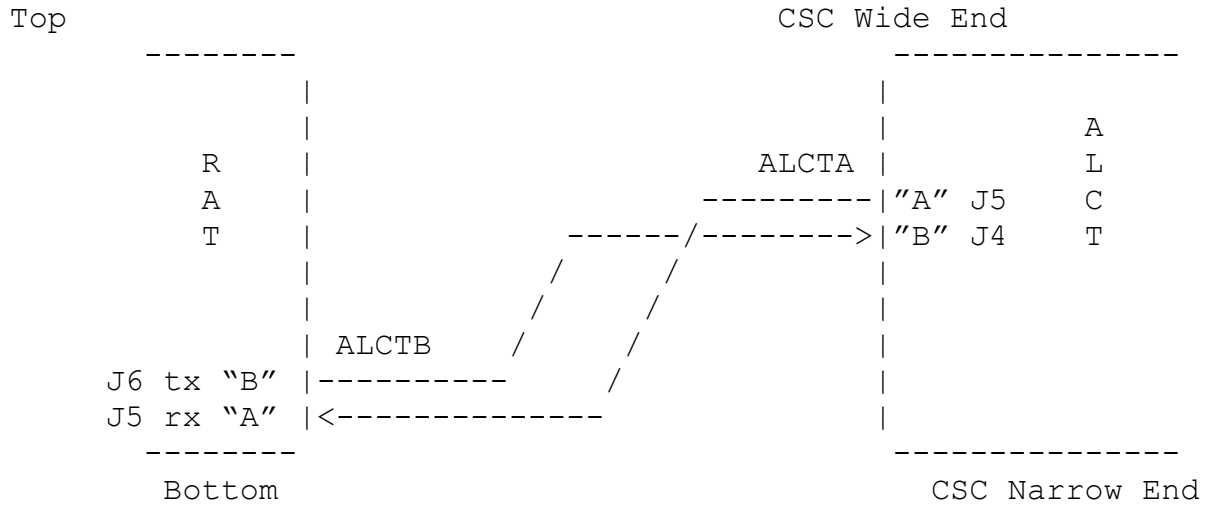
Figure 4: 50 Pin PCB Connector Pin Convention

(Looking At Top of PCB)



² Copied from CFEB design: <http://www.physics.ohio-state.edu/~gujh/works/cmpdata.html>
Page 9 of 13

ALCT Cable Connections



P3B Backplane RPC+ALCT Connector

Function: Sends and receives data to/from ALCT, and receives from RPC.

Connector Type: PCB: AMP Z-Pack 125 (25 rows of 5 pins) female AMP 100145-1
 Backplane: AMP Z-Pack 125 (25 rows of 5 pins) male AMP 188508-9

Table 6: P3B Backplane RPC+ALCT Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	rpc_rx31	B1	rpc_rx30	C1	rpc_rx29	D1	rpc_rx28	E1	rpc_rx27
A2	rpc_rx26	B2	rpc_rx25	C2	rpc_rx24	D2	rpc_rx23	E2	rpc_rx22
A3	rpc_rx21	B3	rpc_rx20	C3	rpc_rx19	D3	rpc_rx18	E3	rpc_rx17
A4	rpc_rx16	B4	rpc_rx15	C4	rpc_rx14	D4	rpc_rx13	E4	rpc_rx12
A5	rpc_rx11	B5	rpc_rx10	C5	rpc_rx9	D5	rpc_rx8	E5	rpc_rx7
A6	rpc_rx6	B6	rpc_rx5	C6	rpc_rx4	D6	rpc_rx3	E6	rpc_rx2
A7	rpc_rx1	B7	rpc_rx0	C7	rpc_clock	D7	smb_clk	E7	tck
A8	tms	B8	tdi	C8	rpc_loop	D8	posneg	E8	sync
A9	tdo	B9	smbrx	C9	rpc_in37	D9	rpc_in36	E9	rpc_in35
A10	rpc_in34	B10	rpc_in33	C10	rpc_in32	D10		E10	+3.3V
A11	+3.3V	B11	+3.3V	C11	GND	D11	GND	E11	GND
A12	alct_rx31	B12	alct_rx30	C12	alct_rx29	D12	alct_rx28	E12	alct_rx27
A13	alct_rx26	B13	alct_rx25	C13	alct_rx24	D13	alct_rx23	E13	alct_rx22
A14	alct_rx21	B14	alct_rx20	C14	alct_rx19	D14	alct_rx18	E14	alct_rx17
A15	alct_rx16	B15	alct_rx15	C15	alct_rx14	D15	alct_rx13	E15	alct_rx12
A16	alct_rx11	B16	alct_rx10	C16	alct_rx9	D16	alct_rx8	E16	alct_rx7
A17	alct_rx6	B17	alct_rx5	C17	alct_rx4	D17	alct_rx3	E17	alct_rx2
A18	alct_rx1	B18	alct_rx0	C18	smbtx	D18	hrst_rpc	E18	free_tx0
A19	alct_oe	B19	alct_clock	C19	alct_clk_en	D19	txoe	E19	alct_loop
A20	alct_tx23	B20	alct_tx22	C20	alct_tx21	D20	alct_tx20	E20	alct_tx19
A21	alct_tx18	B21	alct_tx17	C21	alct_tx16	D21	alct_tx15	E21	alct_tx14
A22	alct_tx13	B22	alct_tx12	C22	alct_tx11	D22	alct_tx10	E22	alct_tx9
A23	alct_tx8	B23	alct_tx7	C23	alct_tx6	D23	alct_tx5	E23	alct_tx4
A24	alct_tx3	B24	alct_tx2	C24	alct_tx1	D24	alct_tx0	E24	+1.8V
A25	+1.8V	B25	+1.8V	C25	GND	D25	GND	E25	GND

PCB Shunts

Table 6: PCB Shunts

Shunt	1-2 Normal Operation Position	2-3 Special Operations
SHP1	Receive RPC0+ bxn[2] on J1 pin 39	Ground J1 pin 39
SHN1	Receive RPC0—bxn[2] on J1 pin 40	Ground J1 pin 40
SHP2	Receive RPC1+ bxn[2] on J1 pin 39	Ground J2 pin 39
SHN2	Receive RPC1—bxn[2] on J1 pin 40	Ground J2 pin 40
SHP3	Receive RPC2+ bxn[2] on J1 pin 39	Ground J3 pin 39
SHN3	Receive RPC2—bxn[2] on J1 pin 40	Ground J3 pin 40
SHP4	Receive RPC3+ bxn[2] on J1 pin 39	Ground J4 pin 39
SHN4	Receive RPC3—bxn[2] on J1 pin 40	Ground J4 pin 40
SH17	Enable FPGA pre-configuration pull-ups	Disable FPGA pre-configuration pull-ups

Revision History

Version	Date	Action
1.00	11/03/2003	Initial
1.00	04/20/2004	Copy from 2003 version