11  Cathode Strip Chamber Local Trigger

11.1  Requirements

The basic criteria for the CSC Local Trigger have been established for some time [11.1]. Because the several megahertz of low-momentum muons produced at full LHC luminosity far exceeds the data acquisition system bandwidth, the Level 1 trigger electronics of the muon detectors of CMS must measure the momentum of penetrating particles using muon system information alone. The muon trigger selection will be on the observed $p_T$, and for a given $p_T$ cut the muon momentum increases as pseudorapidity increases in the forward region. The best trigger momentum measurement comes from combining a vertex constraint with precise measurements of the bend coordinate $(\phi)$ supplied by the CSC Local Trigger in each muon station. The electronics that combine individual station coordinates into tracks and assigns $p_T$, the CSC Track Finder, is described in the following chapter.

The CSC chambers contain six layers of radial cathode strips to precisely measure the $\phi$ coordinate and six layers of nearly orthogonal anode wires whose signals are used to measure the non-bend coordinate $(\eta)$ [11.2]. The CSC cathode strip technique of measuring position by the centroid of charge deposition works better in the presence of high-momentum muon bremsstrahlung than drift-time measuring devices. Another concern for the CSC system, because of its forward location, is the high level of backgrounds expected from punchthrough pions, low-momentum primary muons, secondary muons, and neutron-induced gamma rays. Figure 8.14 shows that the hit rate reaches as high as 500 Hz/cm$^2$ in the innermost portion of ME1/1 and as high as 70 Hz/cm$^2$ elsewhere. The integrated hit rates are as high as 10 kHz per strip and 20 kHz per wire group.

The CSC Local Trigger uses the six-layer redundancy of the CSC chambers to provide precise position information as well as to provide high rejection power against backgrounds. Muon segments, also known as Local Charged Tracks (LCTs) are found in the nearly orthogonal cathode and anode projections by somewhat different algorithms and by different electronic boards. For cathode and anode segments (CLCTs and ALCTs), the number of layers hit and the position and track angle through the chamber is reported. Up to two CLCTs and two ALCTs are found in each chamber during any bunch crossing. The two projections are then combined into 3-dimensional LCTs by timing coincidence. Each correlated LCT then provides to the CSC Track Finder a precision measurement of the bend coordinate $(\phi)$, bend coordinate angle of passage through the chamber $(\phi_b)$, approximate measurement of the non-bend angle coordinate $(\eta)$, and identification of the muon bunch crossing $(bx)$.

The basic design of the CSC Local Trigger electronics is driven by several general performance requirements:

1. Since the CSC Track Finder correlates 2-4 CSC stations, the LCT efficiency must be larger than 95% to have a high overall track finding efficiency. The LCT efficiency can be factored into four largely independent efficiencies: CLCT pattern finding, ALCT pattern finding, ALCT bunch crossing assignment, and ALCT-CLCT time coincidence.
2. The bend coordinate must be measured to an RMS accuracy of 0.15 strips (typically 1 mm), so that the CSC Track Finder can make a meaningful momentum measurement up to 100 GeV/c [11.3].

3. The system must be able to function well in the presence of high anode and cathode background hit rates.

4. The trigger must operate essentially without time.

   There are additional electronics requirements that influence the design:

1. The CSC Track Finder must receive the LCTs by 52 bx, 1.3 µs after the time of primary interaction.

2. The electronics must be able to survive the radiation level in the endcap muon region for 10 LHC years at $10^{34}$/cm$^2$/s luminosity. For electronics mounted on the chambers this is $6.2 \times 10^{14}$ neutrons/cm$^2$ and 1.8 krad of ionizing particles. For electronics mounted on the periphery of the endcap muon iron disks, this is $4.1 \times 10^{10}$ neutrons/cm$^2$ and 0.13 krad of ionizing particles. These estimates are quoted with a factor of three uncertainty.

The design of the CSC Local Trigger has evolved in parallel with the design of the CSC chambers. Therefore, the trigger design makes several requirements on the CSC detectors:

1. The chambers should be able to operate at or above a high voltage corresponding to a minimum ionizing signal charge of 112 fC charge when summed over cathode strips. The preamplifier noise level is approximately 1-2 fC. If the chamber signals are smaller than 50 fC, the momentum resolution of the CSC trigger will be degraded.

2. The CSC chambers should be located with an initial precision better than 1 cm from their nominal positions, in all coordinates, in order to supply a crude muon trigger. The alignment precision required in r-φ coordinates for optimum trigger momentum resolution is 1 mm. The trigger system contains look-up tables to reach this accuracy after some period of analysis of alignment system or muon track data.

3. The time distribution of hits arriving on the anode wires should have an RMS width no larger than 10 ns in order for the multi-layer anode bunch identification algorithm to correctly identify the bunch crossing with high (above 99%) accuracy.

4. The low-voltage power distribution must be designed to avoid over-voltage or under-voltage accidents, due to the inaccessibility of much of the system.

### 11.2 Overview

The Endcap CSC Muon Local Trigger receives signals from front-end cathode and anode electronic boards connected to the Cathode Strip Chambers. Segments of muon tracks are found separately in the nearly orthogonal anode and cathode views. In each view, segment positions, angles, and timing (bunch crossing) are measured. The cathode electronics design is optimized to measure the φ coordinate with high precision, while the anode electronics design is optimized to determine the muon bunch crossing with high efficiency. Cathode and anode segments are correlated in time as well as the number of layers hit. These segments are found in the presence of large background rates from:
1. neutron-induced showers,
2. decay muons, especially at the lowest momenta and in the first muon station,
3. punch-through pions, particularly in the first muon station,
4. primary muons having low energy, and
5. bremsstrahlung showers from the high-momentum muons themselves.

The maximum rate from neutron-induced gamma rays is approximately 10 kHz per strip for cathode hits and 20 kHz per wire group for anode hits. The maximum hit rates from all charged-particle sources are approximately a factor of 10 lower. Simulations indicate that at maximum luminosity, several background clusters exist within each CSC at any given time. To reduce the otherwise huge trigger rate, CSC trigger primitives are formed from tight spatial coincidences of clusters in the 6 chamber layers.

The CSC Local Trigger system selects the two highest-quality LCTs in each CSC chamber and forwards them to the CSC Trigger Track Finder. The CSC Trigger Track Finder operates with a basic segmentation of 60°. The ME1 chambers and outer chambers of ME2-4 cover 10°, while the inner chambers of ME2-4 cover 20°. Figure 11.1 shows how the chamber segmentations are mapped into the CSC Trigger Track Finder segmentation, as well as the 30° sectors (ME1/3 only) for use by the Barrel Track Finder.

The CSC Local Trigger forms LCTs from cathode and anode signals according to the block diagram shown in Figure 11.2. This figure also shows the physical location of each part of the CSC Local Trigger system. The division between the CSC Local Trigger and the CSC Track Finder are the optical links that carry LCT data from the collision hall to the counting room.

The most precise track measurement is obtained by charge digitization and precise interpolation of the cathode strip charges. A simpler and more robust method is used for the CSC local trigger to achieve half-strip localization of the muon track in each cathode layer [11.4]. This is done with a 16-channel “comparator” ASIC that compares the amplified and shaped signals from adjacent strips. If a strip signal is found to be larger than those on its neighbors, a hit is assigned to the strip. Simultaneous comparison of left versus right neighbor strip signals allows assignment of the hit to the right or left side of the central strip, effectively halving the resolution. The six layers are then brought into coincidence in “Local Charged Track” (LCT) pattern circuitry as shown in Figure 11.3. This establishes position of the muon to an RMS accuracy of 0.15 strip widths. Strip widths range from 6-16 mm. Because of the slow 150 ns rise-time of the cathode amplifier/shapers, the cathode electronics does not uniquely identify the bunch crossing.

In the CSC muon system, anode wires are spaced by about 3 mm. The anode wires are hard-wired together (‘ganged’) at the readout end in groups of 10-15 wires to reduce channel count. The algorithm used in determining muon segment position and bunch crossing in the anode view is shown in Figure 11.4. Anode signals are fed into amplifier/constant-fraction discriminators. Since the drift time can be longer than 50 ns, a multi-layer coincidence technique in the anode LCT

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1. Large numbers of neutrons over a broad range of energy are produced from secondary hadronic interactions in the forward region of CMS. These neutrons induce nuclear reactions that produce photons. These photons in turn create electrons that deposit energy in the CSC gas.
pattern circuitry is used to identify the bunch crossing. For each spatial pattern of anode hits, a low coincidence level, typically 2 layers, is used to establish timing, whereas a higher coincidence level, typically 4 layers, is used to establish the existence of a muon track.

The CSC Local Trigger electronics system consists of seven types of boards:

1. **CFEB** - Cathode front-end boards. These boards amplify the cathode signals. After amplification, the CFEB boards contain parallel and independent trigger and precision charge readout data paths. In the trigger path, the positions of charge clusters (hits) are digitized in units of one-half of a cathode strip per plane at the 40 MHz LHC frequency. These hits are compressed by a factor of four and sent to the CLCT/TMB boards described
below. (In the precision charge readout path [11.5], charge is stored in switched capacitor arrays until a Level 1 Accept signal is received, and then the charges are digitized using 12-bit 20-MHz ADCs.)
2. AFEB - Anode front-end boards. These boards contain a combined amplifier/constant fraction discriminator ASIC to digitize the anode information. The anode hits are sent to the ALCT boards described below.

3. ALCT - Anode LCT-finding boards. These boards latch the anode hits at 40 MHz, find hit patterns in the six-layer chambers that are consistent with having originated at the bunch crossing point, and determine the muon bunch crossing by a multiple-layer coincidence timing technique. Up to two anode LCTs can be found per chamber. The anode LCT information is sent to the CLCT/TMB board described below.

4. CLCT/TMB - a combination of Cathode LCT-finding circuits plus Trigger Motherboard circuits. The CLCT section of these boards decodes the pattern of cathode hits from the CFEBs, and finds half-strip hit patterns in the six-layer chambers that are consistent with high-momentum muon tracks. The TMB section of these boards performs a time coincidence of anode and cathode LCT information, and when a coincidence is found, sends the information to the MPC board described below. The TMB selects up to two LCTs based on quality cuts. The TMB may perform a coincidence of LCT positions with RPC hits to reduce the likelihood of ‘ghost’ hits in the case that two or more LCTs are found. Upon receipt of a Level 1 Accept signal (L1A), the anode LCT, cathode LCT, and raw hits information is sent through FIFOs to the DAQMB board described below.

5. MPC - Muon Port Cards. Each MPC receives the LCTs from all of the CLCT/TMB cards in one sector of one endcap muon station, selects the three ‘best’ LCTs, and sends them over optical fiber links to the CSC Track Finder electronics located in the CMS counting room.

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Fig. 11.4: Anode LCT formation from wire group hits (left), and bunch crossing assignment based on numbers of hit layers (right).
6. DAQMB - Motherboards with DAQ interfaces. These boards are part of the trigger system in the sense that they record the anode and cathode LCT and raw hits data in the case of a Level 1 Accept signal (as well as recording the precision charge/position information). The DAQMB sends the data over optical fiber links to the CSC muon system Detector-Dependant Unit (DDU) located in the CMS counting room.

7. CCB - Clock and Control Boards. These boards are the interface from the global CMS Trigger, Timing, and Control (TTC) system [11.6] to the CSC muon system, distributing those signals which are required for operation of the CSC electronics.

Figure 11.5 shows the physical organization of the system. The CFEB, AFEB, and ALCT boards are mounted on the chambers, while CLCT/TMB, MPC, DAQMB, and CCB boards are housed in crates mounted around the periphery of the endcap iron disks.

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**Fig. 11.5:** Physical layout of the CSC trigger electronics.

There are 4 or 5 CFEB boards on each chamber, except for ME1/1 where there are 8. Each CFEB receives inputs from 96 cathode strips. There are 18, 24, or 42 AFEBs per chamber, corresponding to chambers that have 48, 64, or 112 wire groups per plane. Each AFEB receives input signals from 16 anode wire groups. There is one ALCT mounted on each chamber. The on-chamber CFEB and ALCT boards are mounted on the side of the chamber away from the iron disk to which the chamber is attached. The small AFEB boards are plugged into connectors on one edge of the chambers, close to the anode wires. Halogen-free twisted-pair cables carry discriminated signals from the AFEB to the ALCT boards using differential LVDS signal levels.

There is one CLCT/TMB and one DAQMB per chamber. These are located in crates mounted on the periphery of the endcap iron disks. Trigger signals from the on-chamber CFEB and ALCT are sent on high-quality (low-skew) cables to the front panel of CLCT and DAQMB boards located in the peripheral crates. Each peripheral crate services eight (ME1) or nine (ME2-4) CSC chambers. Each peripheral crate services 20° in φ in ME1 and 60° in ME2, ME3, and ME4. There is also one CCB, one MPC, and a VME controller in each CSC peripheral crate. The CCB receives clock and control signals from the TTC system [11.6] and distributes them on a custom backplane within a peripheral crate. The custom backplane is also used for data transfer from CLCT/TMB modules to the DAQMB modules, and from CLCT/TMB modules to the MPC module. A possible layout of a peripheral crate is shown in Figure 11.6: each chamber is serviced by a CLCT/TMB boards paired with a DAQMB board. The central functions of the CCB and MPC modules are...
reflected in the central locations of these modules within the peripheral crates, which minimizes signal propagation delay times and total signal routing length on the custom backplane.

11.3 Cathode Signal Processing

11.3.1 Amplification and Shaping

Each CFEB board reads out 96 cathode strips, arranged 16 strips wide by 6 layers deep. Halogen-free twisted-pair cables carry cathode signals from the edge of the chamber to the CFEBs mounted nearby on the surface of the chamber. The input cathode signals are sent into 16-channel amplifier-shaper ASICs. Each input signal is amplified and shaped into pulses having peak voltage approximately 100 mV per MIP (minimum ionizing particle) for a typical chamber gain of $10^5$. To optimize high-rate performance, circuits to cancel the long tail of the chamber pulse due to ion drift are integrated into the shaper. The output pulse shape is semi-Gaussian. The peaking time and the time for return to baseline with chamber pulse inputs are each about 150 ns. One output of each preamp/shaper channel is connected to a switched capacitor array for storage before possible precision digitization by a commercial ADC. The other output is connected to the trigger path which uses a comparator-network ASIC to digitize the CSC trigger cathode signals. The shaper output signals corresponding to cathode strips at the edge of CFEB towers are sent to adjacent

Fig. 11.6: Slot assignments in a CSC electronics crate mounted on the periphery of the endcap iron disk.
CFEB cards to allow the comparator-network ASIC to function in a seamless manner. Channel by channel gain calibration is done using a set of precisely matched capacitors that couple a test pulse to each input channel. Four levels of charge injection are available under programmable control for each strip. No calibration procedure is required for the cathode trigger.

11.3.2 Trigger Digitization

In CSC chambers, charge collected on the anode wires produces an opposite-sign signal on several strips. For precision track measurement, the position is determined by precise interpolation of the cathode strip charges. For the CSC local trigger, a simpler and more robust method is used to gain somewhat coarser resolution. A threshold is applied to determine strips containing significant charge depositions. The threshold voltage is set by a JTAG-controlled DAC. The trigger position is determined to one-strip width accuracy by determination of the strip with maximum signal. A further factor of two improvement to half-strip accuracy is gained by comparison of signals from the adjacent strips. Were this determination to be perfect, the RMS position resolution would be \( 0.5 / \sqrt{12} = 0.144 \) strip widths, or about 1.5 mm per layer for a typical cathode strip width of 1.0 cm. These comparisons of strip charges to threshold and to each other are accomplished in the comparator-network ASIC as shown in Figure 11.7: the pulse from the preamp/shaper for strip \( N \) is compared to a pre-set threshold level and compared to pulses from neighboring strips (strip \( N-1 \) and strip \( N+1 \)). Strip \( N \) has the peak charge if its pulse is larger than all three. The track hit position is localized to either right or left half of strip \( N \) by a fourth comparator which compares pulses from strip \( N-1 \) and strip \( N+1 \). The output levels from the comparators are fed into AND gates and latched to produce two digital signals \( L_N \) and \( R_N \) indicating hits on strip \( N \) left or right side, respectively.

![Comparator-network ASIC block diagram.](image)

**Fig. 11.7:** Comparator-network ASIC block diagram.

The comparator ASIC receives inputs from 16 strips plus two additional neighbor strips. The signal is compared to threshold every clock cycle. After the signal first exceeds the threshold, a programmable delay (typically 150 ns) allows the cathode signals to reach their peaks. After this delay, the strip signal is compared to neighbor signals. The slow control system is used to select the operating mode for the comparator ASICs and to set the threshold DAC. A JTAG link from the
DAQMB writes three CFEB register bits that select the comparator's peaking time of 25 ns to 200 ns in 25 ns steps. In addition, two register bits select one of three possible trigger modes. Mode 0 requires the preamp/shaper output voltage to be above threshold for only one clock. Mode 1 requires that the voltage still be above threshold after the peak delay time. Mode 2 requires that the voltage remain above threshold for every clock cycle up to and including the peak delay time.

Half-strip localization errors occur for 10-20% of hits, partly due to analog circuit noise and partly due to the presence of delta rays and muon bremsstrahlung. In all but about 2% of the hits, the discrepancy is limited to one half-strip width.

Internally, 32 half-strip bits are produced by the comparator ASIC. Digital circuitry in the comparator ASIC compresses the 32 half-strip bits into 8 output time-sequenced “di-strip triad” bits. This is accomplished in lossless fashion because of two facts. First, the comparison of neighbor strips to find the charge maximum only allows one of two adjacent strips to produce a half-strip bit at any one time. Second, the shaper signals develop slowly compared to the bunch crossing time. The output triad bits come from the comparator ASIC at 40 MHz, thus taking 75 ns compared to the preamp/shaper return to baseline time of about 150 ns. The first triad bit indicates the presence of a hit on one of two adjacent strips, the second indicates which of the two strips contains the hit, and the third bit indicates whether the hit was located on the left or the right side of the strip.

The digitization circuitry of the comparator ASIC can be controlled by several input lines. The “peaking” time delay between the first observation of a signal over threshold and the comparison of neighbor strips can be adjusted between 1 and 8 clock cycles (25 ns to 200 ns). The signal can be required to exceed threshold in three modes: only at one clock cycle, at each clock cycle up to the “peaking time”, or at the first clock cycle plus the cycle at the “peaking time”.

Analog and digital signals are sent between adjacent CFEB boards in order to perform seamless cluster finding across board boundaries. Six analog signals (one for each layer) are sent to neighboring boards on each side, and six analog input signals are received. These are in pairs that alternate signal with ground. Digital signals are needed as “carry” bits for the cluster finding logic. Carry bits are received from the left-adjacent board (which has lower strip numbers), and transmitted to the right-adjacent board (higher strip numbers). LVDS drivers and receivers are used to minimize noise.

The six comparator ASICs on each 96-channel CFEB card produce 48 single-ended output bits at 40 MHz. This data is fed into serializers that convert the data to a higher bit rate and send it out as differential LVDS signals, including a clock signal which is carried with the data. A low-skew output cable brings these signals to the CLCT boards located in crates mounted on the periphery of the endcap iron disks. The links also send their own ID number (0 or 1) and a “Link Alive” bit that indicates the CFEB is powered up. The cable also contains two signals that are not fed through the bit serializers: the 40 MHz strobe sent to the CFEB board in order to clock the digital portions of the comparator ASICs, and a reset signal.

11.3.3 Cathode LCT Pattern-Finding

A muon passing through a CSC chamber will produce distinctive patterns of half-strip hits in the six-layer endcap muon CSC chambers. By identifying these patterns, the CSC Local Trigger provides high rejection power against backgrounds. The largest background source, neutron-induced gamma ray conversions, are generally low in energy, and produce mostly single-
layer or short multi-layer hits. Other backgrounds, such as low-momentum muons or punch-through particles often do not point well enough to the primary interaction region to be considered high-momentum muon candidates. The six-layer correlation can allow for half-strip location errors. These errors occur for 10-20% of hits, partly due to analog circuit noise, and partly due to the presence of delta rays and muon bremsstrahlung. The six-layer correlation also provides somewhat improved position resolution and provides a rough measurement of the bend angle ($\phi_b$) within the approximately 15 cm path length between the first and the sixth plane of the chamber.

Patterns are found within half-strip patterns for tracks with $p_T > 10$ GeV/c in ME1 and all tracks in ME2, ME3, or ME4. Low-momentum tracks (2.5 < $p_T < 10$ GeV/c) in ME1 bend the most, requiring an additional set of di-strip patterns. In ME1, where muon tracks have the largest curvature, a minimum number of layers (usually 4) with hits is required within the envelope of half-strip or di-strips shown in Figure 11.8. The envelope used in other stations is in general narrower, and depends on the station number and whether it is an inner or an outer CSC chamber. If gate array technology improves substantially by the time that CLCT implementation is frozen, more specific envelopes can be defined and a somewhat improved position resolution can be obtained.

![Fig. 11.8: The envelope of cathode half-strip or di-strip hits used in CLCT pattern-finding.](image)

On the CLCT/TMB board, inputs from the comparator ASICs are de-serialized and converted from differential LVDS to single-ended TTL levels. The clock signals returned with the comparator data from the CFEBs are synchronous with the LHC clock, but have different phases than the TMB/CLCT board clock. These phases depend on the lengths of cables between the CFEB and CLCT/TMB boards and may be inconvenient for reliable latching in the CLCT ciriucity. Therefore, synchronization of the input comparator data on a time scale finer than one bunch crossing is necessary. A simple circuit eliminates the possibility of unreliable data reception from the CFEB. This circuit latches input comparator data on both rising and falling edges of the on-board clock. Then a programmable multiplexer selects the more favorable phase. Finally, a latch having a setup and hold time of less than one-half of a clock cycle stores the data on the rising edge of the on-board clock signal.
The comparator signals are then fed into one large field-programmable gate array (called variously FPGA or PLD, depending on the manufacturer) per CSC chamber. Hot or dead comparator di-strip channels can be masked on input to this device. The gate array performs the cathode segment-finding (CLCT) function shown in Figure 11.9. The CLCT gate array decodes the sequential comparator ASIC triad bits into up to 240 internal di-strip bits and up to 960 half-strip bits. The bits are “stretched” to a length such as 75 ns which allows for coincidence between layers in the presence of varying drift times. These bits are fed into the LCT trigger processor which look for multi-layer coincidences within predetermined patterns. The magnetic field in the endcap causes bending of charged tracks in the azimuthal direction, transverse to the strips. In the first muon station, high $p_T (>10$ GeV/c) tracks bend a maximum of 1.8 strips in the 15 cm between the first and sixth layer in the chamber. Low $p_T (2.5-10$ GeV/c) tracks will bend as much as 7.2 strips in the chamber. The amount of bending is much less in the other endcap muon stations.

An $n$-layer ($1 \leq n \leq 6$) coincidence within the envelope of di-strips shown in Figure 11.8 gives a pre-trigger indication. Typically, $n=2$. When a pre-trigger is found, a time delay such as 50 ns is taken to allow long-drift time hits to arrive. Then an LCT is found using restrictive $m$-layer ($1 \leq m \leq 6$) patterns among the half-strip bits. Typically, $m=4$. Each pattern has an 8-bit pattern number. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit. Muon stubs that overlap two CFEBs are recognized as a single stub. If more than one stub is found within 16 adjacent strips, a priority encoder on the output of the pattern-finding circuitry selects the single best cathode LCT according to the pattern number. If more than two cathode LCTs are found within the entire chamber, the best two are retained according to the pattern number. For diagnostic purposes, the raw comparator bits can be stored in a pipeline and frozen when a CLCT is found, for later serial readout through the DAQ chain. This readout is initiated by reception of L1A for the appropriate bunch crossing.

Data for each cathode LCT is sent to the TMB according [11.7] to Table 11.1. The “Valid Pattern flag” indicates a valid LCT pattern has been found and information is being sent on the current clock cycle. The 8-bit pattern number encodes the number of layers, the pattern of half-strips or di-strips found, and whether the pattern consists of half-strips or di-strips. The bend bit indicates whether the track is heading towards lower or higher strip number. Although the half-strip and di-strip patterns can be distinguished by pattern number, a separate bit to distinguish these cases is sent for ease of decoding. For high $p_T$ patterns, the 8-bit half-strip ID is between 0 and 159. For low $p_T$ patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber. It should be noted that this does not require a hit to have actually been registered in the third chamber layer. Finally, the 5 low-order bits of the bunch crossing number to which the cathode LCT data is associated is sent for timing verification.

### 11.4 Anode Signal Processing

The anode trigger is designed to optimize the muon bunch crossing identification. Each input channel of the AFEB is a ganged group of wires (10 to 20) from a layer. The AFEB cards amplify and discriminate the anode signals and send logic pulses when anode signals exceed a predetermined threshold.

Logic pulses from the AFEB discriminators are sent by differential LVDS to a single on-chamber ALCT board which finds track segments and determines the bunch crossing time of
the track segment. Although the drift time distribution in CSC chambers has a small but long tail beyond 50 ns, the correct 25 ns bunch crossing can be identified with high efficiency by a coincidence technique. The ALCT board latches the anode wire group hits at 25 ns intervals, and identifies the bunch crossing from the first $n$-layer ($1 \leq n \leq 6$) coincidence of hits. Test beam studies show that once the system is properly timed any choice of multiplicity within $1 \leq n \leq 4$ yields a bunch crossing tagging efficiency in excess of 99%. The optimum phase of the 25 ns coincidence window depends on the required multiplicity. Although a 1-fold coincidence level produces high efficiency in the absence of backgrounds, it is susceptible to being fooled by early signals from the high rate of neutron-induced background hits, and higher coincidence levels are preferred.

**Fig. 11.9:** CLCT block diagram, including input data decoding, pattern lookup, pattern selection, trigger output formatting, and DAQ diagnostic data recording.

**Table 11.1:** CLCT output bits to Trigger Motherboard.

<table>
<thead>
<tr>
<th>CLCT Output Data</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid Pattern flag</td>
<td>1</td>
</tr>
<tr>
<td>Pattern number (0-255)</td>
<td>8</td>
</tr>
<tr>
<td>Bend left/right (0/1)</td>
<td>1</td>
</tr>
<tr>
<td>Half or Di-strip pattern flag (0/1)</td>
<td>1</td>
</tr>
<tr>
<td>Half- or Di-strip ID (0-159, 0-39)</td>
<td>8</td>
</tr>
<tr>
<td>bx low-order bits</td>
<td>5</td>
</tr>
<tr>
<td>Total</td>
<td>24</td>
</tr>
</tbody>
</table>
The \( n \)-layer coincidence that identifies the bunch crossing also serves as a pre-trigger indication. Like the CLCT board, after a pre-trigger is found, a time delay such as 50 ns is taken to allow long-drift time hits to arrive. Then an LCT is found using restrictive \( m \)-layer (\( 1 \leq m \leq 6 \)) patterns among the wire group bits that are consistent with coming from the primary interaction. Typically, \( m=4 \).

The ALCT board sends data for up to two muon track segments to the CLCT/TMB board mounted in the peripheral crates, which forms a coincidence between anode and cathode LCTs. For diagnostic purposes, the ALCT muon stub information and the discriminator output pulses are latched and pipelined for readout into the DAQ system, providing hit/no-hit information for each of the wire groups. The connection to the DAQ system is provided through a cable to the CLCT/TMB module.

### 11.4.1 CSC Anode Digitization

Each AFEB card contains one 16-channel preamplifier-shaper-discriminator ASIC. The small AFEB cards are mounted on the sides of the CSC chambers close to the anode wires in order to minimize input signal path length and thus noise levels. Typical thresholds are 20 fC, while a MIP signal exceeds 100 fC. The anode amplifiers are similar to the ones on the CFEB boards, but optimized for the summed anode input capacitance and shaped with a peaking time of 30 ns. The amplifier outputs are sent into constant-fraction discriminators. Time walk between 20 fC and 100 fC levels is observed to be less than 4 ns. The output stage produces logic pulses with a minimum width of 35 ns and a maximum width equal to the time over threshold. The logic pulses are sent from AFEB cards to the on-chamber ALCT board using differential LVDS levels. The AFEB cards accept an analog test pulse input from the ALCT that is fed to the input of all amplifier channels simultaneously. Power levels of +5.5V and (in the case of ME1/1) -4.3V are required. The AFEB cards also accept a “stand-by” level that can be used to disable the ASIC, for instance, in case of latch-up. A single 40-pin cable between the ALCT and each AFEB carries the 16 differential discriminator output signals, power levels and ground, the threshold level, test pulse, and stand-by level.

### 11.4.2 Anode LCT Pattern Finding

LCT trigger patterns among a set of hits in anode wire groups are found in the same way as those for the strips. Here the segmentation is much coarser and the roads are straight lines to the interaction region, independent of \( p_T \). The roads differ across a chamber due to the changing polar angle. The anode patterns are found within the envelope of wire group hits shown in Figure 11.10.

The functional diagram for the anode trigger is shown in Figure 11.11. Within each road, the number of layers containing hits is counted on every bunch crossing. Two programmable layer-coincidence levels are employed. When the pre-trigger level is exceeded, the bunch crossing time is identified and a fixed delay, such as 50 ns, is imposed to wait for long-drifting anode hits. After the delay, if the second coincidence level is exceeded, the muon track position is defined.

Each pattern has a 2-bit pattern number. Higher pattern numbers are assigned to ALCTs with more layers hit. If more than one stub is found within 16 adjacent wire groups, a priority encoder on the output of the pattern-finding circuitry selects the single best ALCT according to the pattern number. If more than two anode LCTs are found within the chamber, the best two are
retained and sent to the TMB according to the pattern number. For diagnostic purposes, the wire hit bits are stored in a pipeline and frozen when an ALCT is found for later serial readout through the DAQ chain. This readout is initiated by reception of L1A for the appropriate bunch crossing.

On the ALCT board, inputs from the anode preamplifier/discriminator ASICs are converted from differential LVDS to single-ended TTL levels in custom 16-channel delay ASICs. The delay ASIC delays the anode signals over a range of 32 ns in 4 ns steps, depending on 3-bit control inputs. The fine delay control changes the phase of the anode signals with respect to the LHC clock used for latching the anode signals. This is necessary to get optimum bunch crossing tagging efficiency. The delayed anode discriminator signals are then fed into field-programmable gate arrays that perform the anode segment-finding (ALCT) function.

Hot or dead anode channels are masked on input to the pattern-finding FPGAs. The anode bits are then stretched to a duration, such as 75 ns, that allows for coincidence between layers in the presence of varying drift times. These bits are fed into the LCT trigger processor which look for n-layer coincidences within predetermined patterns.

There are collision muon and accelerator muon ALCT patterns. The collision muon patterns project to the collision point, while the accelerator muon patterns are parallel to the beam axis. It is possible to completely shut off either of these types under software control. The number of layers struck within each pattern (0-6) defines a 3-bit pattern quality number. The pattern type bit (collision versus accelerator) is added to the pattern quality number to make a 4-bit quantity by which patterns are sorted. The pattern type bit is added as the high-order bit, with a software-selectable polarity. In normal operation, the polarity will be set so that collision patterns are represented by a one and thus preferred to accelerator patterns. If more than one ALCT pattern is found within 16 adjacent wire groups, a priority encoder on the output of the pattern-finding circuitry selects the single best pattern according to the pattern number. If two equal pattern numbers are found on different wire groups, then the pattern on the wire group furthest from the beam axis (lowest pseudorapidity) is selected. If more than two ALCT patterns are found within the entire chamber, the best two are retained according to the pattern number.

**Fig. 11.10:** The envelope of anode wire group hits used in ALCT pattern-finding.
Table 11.2 shows the data sent to the TMB for each anode LCT pattern [11.7]. The “Valid Pattern flag” signals that a valid LCT pattern has been found and information is being sent on the current clock cycle. The 2-bit pattern quality number is the number of layers hit minus three. The accelerator muon bit indicates if there were hit patterns that appear to be parallel to the beam axis. This may be used for triggering on accelerator or halo muons, or may be used to veto chambers containing such muons. The latter capability could be useful if the rate of these muons is higher than anticipated. The 7-bit wire group ID number indicating the position of the pattern within the chamber runs 0-111. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber. This does not require a hit to have been registered in the third chamber layer. Finally, the 5 low-order bits of the ALCT bunch crossing number is sent to the TMB for timing verification.

Table 11.2: Anode LCT output to Trigger Motherboard

<table>
<thead>
<tr>
<th>ALCT Output Data</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid Pattern flag</td>
<td>1</td>
</tr>
<tr>
<td>Pattern quality (0-3)</td>
<td>2</td>
</tr>
<tr>
<td>Accelerator muon</td>
<td>1</td>
</tr>
<tr>
<td>Wire group ID (0-111)</td>
<td>7</td>
</tr>
<tr>
<td>bx low-order bits</td>
<td>5</td>
</tr>
<tr>
<td>Total</td>
<td>16</td>
</tr>
</tbody>
</table>

Fig. 11.11: ALCT block diagram, including pattern lookup, pattern selection, trigger output formatting, and DAQ diagnostic data recording.
11.5 Cathode-Anode Correlation

The Trigger Motherboard (TMB) portion of the CLCT/TMB card receives up to two anode stubs from the ALCT board and two cathode stubs from the CLCT portion of the CLCT/TMB card [1]. The functions of the TMB circuitry are:

1. Bunch crossing alignment of the anode and cathode tags.
2. Correlation of the Anode and Cathode LCT words and construction of two combined LCTs.
3. Transmission of LCT data to the Muon Port Card (MPC) for triggering, and transmission of DAQ data to the DAQ Motherboard (DAQMB).

Each of these functions is described in more detail in following sections. A preliminary plan has been developed [11.8] in which a coincidence between the LCT and the RPC information can be made at the TMB. This may allow a reduction in the rate of CSC ghosts in the case of two or more muon candidates in a CSC chamber.

11.5.1 Bunch Crossing Alignment

Incoming anode and cathode LCTs are not aligned in time. Anode LCTs are created faster than cathode LCTs because of the slow development of the cathode preamp signal, and because processing inside the ALCT card is faster than processing inside the CLCT logic. The TMB contains input pipeline logic in order to delay anode LCTs for a programmable number of bunch crossings up to 10.

11.5.2 Cathode-Anode Matching

The anode and cathode LCTs are matched according to the more precise ALCT bunch crossing number (BXN). The Cathode LCT BXN can differ by at most ±1 bunch crossing. For each of the selected muons the TMB outputs a 2-bit bunch crossing match word as shown [11.7] in Table 11.3. These may be used by later boards in the trigger chain if additional quality information is needed. They also allow the analysis of the bunch crossing matching in the TMB, since a large number of bad matches could be an indication of a timing alignment problem.

Table 11.3: Bunch Crossing Match Bits.

<table>
<thead>
<tr>
<th>BXN Match</th>
<th>ALCT BXN - CLCT BXN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>-1</td>
</tr>
<tr>
<td>3</td>
<td>&gt; ±1 (Error)</td>
</tr>
</tbody>
</table>

The ideal case for a high-momentum muon is one anode and one cathode LCT pattern. However, other cases may occur, which are distinguished by a 2-bit “STA” (Status type A) code as shown [11.7] in Table 11.4:
1. The TMB may receive one or two anode LCTs and zero cathode LCT patterns. This happens, for example, for very low-momentum muons. Although the non-zero data is forwarded to the MPC, this case is flagged by STA=1, as is the similar case of one or two cathode LCT and zero anode LCT patterns.

2. If the TMB receives two anode LCTs and one cathode LCT, the TMB outputs two LCTs, by copying the Cathode LCT bits into both muons. These, and the similar case of two cathode LCTs and one anode LCT, are flagged by STA=2.

3. If there are two anode LCTs and two cathode LCTs in one chamber, they are matched according to their pattern numbers: the largest ALCT and CLCT pattern numbers are paired, and the second largest ALCT and CLCT pattern numbers are paired. These, and the ideal case of a single match, are flagged by STA=3.

<table>
<thead>
<tr>
<th>STA value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No CSC trigger data</td>
</tr>
<tr>
<td>1</td>
<td>There is CSC trigger data but no anode-cathode match is found</td>
</tr>
<tr>
<td>2</td>
<td>Two cathode and one anode LCT patterns, or vice versa</td>
</tr>
<tr>
<td>3</td>
<td>One or two LCT patterns, unambiguous assignment</td>
</tr>
</tbody>
</table>

TMBs maintain a local Bunch Crossing Number (BXN) using signals from the Clock and Control Board. The internal BXN is compared to the BXN received from the ALCT module, and the Sync Error bit is set if a mismatch is detected.

11.5.3 LCT Data Transmission to the MPC

The TMB sends up to two anode LCT and two cathode LCT patterns for one CSC chamber to the MPC every 25 ns. The bits are indicated [11.7] in Table 11.5. Some bits are the same for the two muons from one CSC; these are marked with an asterisk in the table. The data is passed on a custom connector backplane. Since 630 bits (data from nine TMBs) are sent every clock cycle, the data is compressed onto fewer backplane lines, using serialization before transmission to the MPC.

11.6 Muon Port Card Selection of LCTs

The high cost of optical links makes it prohibitively expensive to send every LCT from the TMBs to the counting room. Thus, a Muon Port Card (MPC) is used to reduce the data. In each of stations 2, 3, and 4, an MPC receives signals from 9 chambers corresponding to 60 degrees in $\phi$ in one station: three high-$\eta$ 20$^0$ chambers and six low-$\eta$ 10$^0$ chambers. In station 1, an MPC receives signals from 8 chambers corresponding to 20$^0$ in $\phi$: two 10$^0$ chambers in each of four types, the high-$\eta$ and low-$\eta$ sections of ME1/1, plus ME1/2 and ME1/3. Each MPC in stations 2, 3, and 4 reduces the number of LCTs to three or less and sends them to the Sector Receiver (SR) module via optical links. In station 1, the number of output LCTs is two or less.
11.6.1 MPC Functionality

The MPC performs the following functions:

1. Data collection. The MPC receives data from nine TMB every bunch crossing. Each TMB sends up to two LCT patterns. Up to 18 LCT patterns may come to an MPC simultaneously.

2. Synchronization of incoming LCTs with the MPC local master clock.

3. LCT selection. The MPC selects the best three LCTs out of 18 possible, except in ME1 where two LCTs are selected out of 16 possible.

4. Reformatting of the three selected LCTs and their transmission to SRC via optical links.

11.6.2 MPC Input Synchronization

When the LCTs are sent from the TMB to the MPC, they have a phase shift with respect to the local clock at the destination, and must be synchronized. The local 40.08 MHz master clock at the MPC is sent from the Clock and Control Board. Also, there are 18 bunch crossing counts
accompanying the LCTs. These will be compared to the Port Card bunch crossing counter to detect errors. For the bunch crossing synchronization we propose to use pipeline shift registers on the inputs of LCT logic.

11.6.3 Selection Logic

Flexible selection logic is based on Look-Up Table (LUT) conversion. In this case the Pattern IDs from all incoming LCTs serve as addresses for the LUT, and the LUT output represents a quality factor corresponding to a particular combination of wire and strip patterns. Presently we are allowing up to 11 bits to be used to address the memory, of which the lower 8 bits are the CLCT pattern number and two higher bits are the ALCT quality number. One bit is unassigned. The LUT output is currently an 8 bit floating point number representing the product of the two pattern id’s. The output of the LUT is arbitrary and reprogrammable allowing us to modify the function as we gain experience under real running conditions.

11.6.4 Interface to Sector Receiver Card

The distance between on-chamber electronics (FEBs, MBs, MPC) and the counting room is about 100 m. The MPC must be able to transmit 120 bits of data every 25 ns. Optical links are the best and possibly the only choice for communication between MPC and SRC. The general requirements for these optical links are:

1. Simplex links
2. 25 ns framing.
3. Simple error detection, no error correction.
4. Effective bandwidth of 1 Gbit/s, or 25 bits per bunch crossing.

Each MPC contain parallel to serial converters and optical transmitter modules, while each Sector Receiver (SR) contains optical receiver modules and serial to parallel converters. For prototyping purposes we have been using the Hewlett Packard HDMP-1022/1024 Transmitter/Receiver chip set. This chip set has user-selectable parallel data widths (16, 17, 20, or 21 bits) and high-speed serial data rates. To transmit 120 bits of data at 40 MHz using a 20-bit data width, we need six transmitters on each MPC, six optical modules, and six optical fibers. This chip set has relatively high power consumption and high price. We are currently prototyping with this chip set. Other chip sets will be evaluated in the coming year, including the Texas Instruments TLK2500/2501 chipset running at 80 MHz.

11.7 Clock and Control Board

CSC Clock & Control Boards (CCBs) receive timing information from the LHC accelerator Timing, Trigger, and Control (TTC) system [11.6]. One CCB resides in each detector-mounted peripheral crate to distribute the 40 MHz system-clock to the ALCT, CLCT, DAQMB, and TMB modules. The backplanes and CCB modules are designed to account for path-length delays so each trigger module receives the clock at the same point in time.

Clock, bunch-crossing-reset, and bunch-crossing-zero signals are distributed from the CCB to the trigger modules, instead of sending the bunch crossing number. Each trigger module
that needs the BXN will maintain an internal counter that increments every clock cycle. When a
bunch-crossing-reset signal arrives, the counter halts, and resets to its initialization value. Counting
resumes when the bunch-crossing-zero signal is received.

Additional CCB signals that may be needed by peripheral crate electronics to mitigate
radiation upsets (SEU), such as CSC logic resets, are under discussion.

### 11.8 Synchronization and Latency

The source of clock signals for the CSC Local Trigger are TTCrx [11.6] receivers; one
is mounted on each CCB card, i.e., one per peripheral trigger crate. The CCB card has been
designed to deliver isochronous clock signals to each occupied slot of these crates. Each CLCT/
TMB card distributes the clock signal to the on-chamber trigger cards, i.e., one ALCT card and up
to five CFEB cards.

The return trigger data signals will arrive at the CLCT/TMB board with an arbitrary
phase relative to the CLCT/TMB on-board clock due to chamber-to-chamber variations in the
connecting cable lengths. Since these signals might lie within the setup and hold time of the input
latches and not be reliably latched, phase adjustment in several steps within the 25 ns cycle will be
provided for the clock signals from CLCT/TMB to the on-chamber trigger cards.

The timing of the anode hits relative to the LHC clock with which they are latched needs
to be adjusted within ±2 ns to obtain the optimum probability for identifying the muon bunch
crossing. Muons have times of flight to the various endcap chambers that vary from 19-42 ns.
Within a single chamber the time of electrical signal propagation varies by as much as 9 ns due to
different wire lengths and cable lengths from front-end anode boards to the ALCT board.
Therefore, the fine timing needs to be adjusted within each chamber. This is done on the ALCT
card by 16-channel ASICs that delay the signals by 0-30 ns in 2 ns steps. These chips also shift
differential LVDS signals to TTL levels.

No comparable provision is made for fine timing of cathode comparator signals, since
the CLCT timing requirement is imposed as ±1 bx by the anode/cathode time coincidence at the
TMB. However, since the ALCT data is ready well before the CLCT data, the ALCT information
is delayed by an integer number of crossings in the TMB in order to bring both types of LCT data
into time coincidence.

The bunch crossing number BXN is calculated on the ALCT, CLCT/TMB, and MPC
boards. In each case, the calculation is done using BxReset and BC0 pulses distributed from the
CCB board. The BxReset pulse stops a 12-bit (0-3563) bunch crossing counter and loads it with a
pre-determined offset value. Counting resumes from the preset values with the arrival of the bunch
zero (BC0) pulse. The ALCT, CLCT/TMB, and MPC modules have appropriate BXN preset
values that compensate for their different processing times so that their BXNs for a given muon
will match. At each stage, the low-order bits of BXN are compared to ensure synchronization.
Errors are handled by zeroing output data and recording the discrepancy for DAQ readout.

MPC optical link synchronization is handled by the Sector Receiver and is described in
the following chapter.
11.8.1 Synchronization Procedure

The Anode LCT is used to synchronize the trigger system. The Anode LCT identifies the correct bunch crossing with greater than 99% efficiency. The BXN generated by the ALCT will be histogrammed and compared to the bunch crossing structure of the LHC beam. By using the repeating nature of the bunch structure, the ALCT synchronization can be determined from the CSC data in 25 minutes of running at $10^{32}\text{cm}^{-2}\text{s}^{-1}$. Each board in the CSC trigger chain counts BXN starting from its preset value and sends BXN on the output trigger link. This makes it possible to determine the offsets for the other boards in the CSC trigger system.

11.8.2 TMB Synchronization of ALCT Data

On the CLCT/TMB module, the ALCT data is first de-serialized. Although the incoming data clock is synchronous to the LHC clock, it will have a different phase from the TMB/CLCT board clock, depending on the length of cables between the ALCT and CLCT/TMB boards. This phase can be inconvenient for reliable latching in the TMB circuitry. Therefore, synchronization of the input ALCT data on a time scale finer than one bunch crossing is necessary. A simple circuit eliminates the possibility of unreliable data reception from the ALCT. One possible circuit latches input ALCT data on both rising and falling edges of the on-board clock. Then a programmable multiplexer selects the more favorable phase. Finally, a latch having a setup and hold time of less than one-half bunch crossing stores the data on the next cycle on the rising edge of the on-board clock signal.

11.8.3 Latency Determination

The estimated latency of the CSC Local Trigger is 51.5 bx, from the time of the collision until data is available at the end of the optical fiber in the counting room. This, plus the latency of the CSC Track-Finder, is sufficient to furnish CSC trigger data to the Global Muon Trigger 78 bx after the collision. The accounting of this latency, with emphasis on the critical path cathode signals, is shown in Table 11.6.

<table>
<thead>
<tr>
<th>Description</th>
<th>bx this step</th>
<th>Total bx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time of Collision</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>Time of flight and signal propagation</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Cathode preamp peaking time and latency</td>
<td>6.0</td>
<td>8.0</td>
</tr>
<tr>
<td>Comparator latency plus signal transmission to CLCT/TMB</td>
<td>5.0</td>
<td>13.0</td>
</tr>
<tr>
<td>Logic to find Anode and Cathode LCTs and combine them</td>
<td>15.5</td>
<td>28.5</td>
</tr>
<tr>
<td>Port Card processing</td>
<td>5.0</td>
<td>33.5</td>
</tr>
<tr>
<td>Optical link transmission (90m)</td>
<td>18.0</td>
<td>51.5</td>
</tr>
</tbody>
</table>
11.9 Prototypes

Electronics prototypes were tested on full-size prototypes of the largest CSC chamber in the summers of 1998 and 1999 at CERN [11.9]. The first tests in 1998 were done at the H2 beam line, where a silicon beam telescope was used for resolution studies. Later tests in 1998 and 1999 were done at the GIF (Gamma Irradiation Facility), where LHC-like backgrounds were provided by an intense gamma source. The main purpose of the 1998 tests was to verify the performance of the CSC trigger electronics, while the main purposes of the 1999 tests were to test performance under high background rate conditions and verify engineering features such as large count and serial DAQ readout through a DDU.

Prototype comparator ASICs were produced in 1997, 1998, and 1999. Prototype ALCT and CLCT boards were produced in 1998 and 1999, and an additional ALCT prototype was produced in 2000. Near-final prototypes exist for all on-chamber CSC system electronics (CFEB, AFEB, and ALCT boards). These boards have been successfully radiation-tested during 2000.

Off-chamber CSC local trigger-related electronics (CLCT/TMB, MPC, DAQMB, and CCB boards) have been successfully prototyped but not finalized.

11.9.1 Comparator ASIC Prototypes

The 16-channel cathode comparator ASICs tested during summer 1998 had 32 half-strip output bits. Six of these chips were mounted on a 96-channel comparator board, shown in Figure 11.12, that attached directly through connectors to the cathode front-end board. The 192 half-strip bits were converted from TTL levels to differential LVDS and 96 of these signals were driven on cables to a cathode LCT card in a CAMAC crate, where they were recorded. From the 1998 data, the efficiency of the comparator ASICs for identifying the correct half-strip was determined in two ways. First, the half-strip bits were compared to bits predicted by the precision charge determination of the front-end DAQ cards [3]. These cards employ switched-capacitor arrays (SCAs) for charge storage and ADCs for digitization. The typical noise level on the DAQ data was 1.6 fC (1.6 mV after the amplifier/shapers), while the typical total cathode charge was 100 fC. The efficiency was found to be 90.4±0.2% for exact half-strip match, while a match window of ±1 half-strips yielded an efficiency of 98.3±0.1%. The second way the comparator match efficiency was determined is less biased but gives lower statistics. This method uses the precision DAQ data to track muons through the chamber, leaving out one layer (#3) from the fit. The extrapolated position in this layer is then compared to the half-strip bit found by the comparator ASIC. By this method, the efficiency for exact half-strip match is measured to be 88.2±0.7%, while a widened match window of ±1 half-strips yields an efficiency of 94.9±0.4%.

Digital circuitry in the 1999 version of the comparator ASIC compresses the 32 half-strip bits into 8 output time-sequenced “di-strip triad” bits. An entire set of these ASICs for one entire full-size CSC chamber was tested during the summer 1999 test beam studies. Performance was similar to that of the 1998 Comparator ASIC, while the 4:1 compression plus the use of bit serializers resulted in a much higher ratio of channels to signal cables.

11.9.2 Cathode LCT Prototypes

In the 1998 tests, the half-strip bits found by the comparator ASICs were sent to a 48-strip cathode LCT card, which identified the multi-layer patterns of valid muon trajectories. All
ideal patterns of muon tracks within the envelope shown in Figure 11.8 were included. A mezzanine card converted LVDS signals to TTL levels. These signals were distributed by a “front” Altera 10K50 PLD (programmable logic device) to Cypress 128Kx8bit SRAMs, which found the patterns, while a “rear” Altera 10K20 PLD collected the patterns (if any) found by the SRAMs and selected the best according to pattern number. Higher numbers corresponded to larger numbers of hit layers and straighter tracks. The CAMAC interface was implemented in another Altera 10K20 PLD. Output trigger information was fed through a National Instruments Channel-Link to a “Trigger Motherboard” which sorted LCTs in the case of multiple candidates, and performed a time coincidence between cathode LCTs and anode LCTs. These modules are shown in Figure 11.13, running in internal trigger mode at the H2 beam line.

The efficiency of the cathode LCT card for identifying muons was measured both by comparison with the precision DAQ data, and by comparison to external muon tracking provided by a silicon telescope. The position reported by the cathode LCT card corresponded to the track position at chamber layer 3. When DAQ data was found in layer 3, the position of the cathode LCT was compared to the layer 3 cluster center. Of these events, 95% were found as half-strip (high-momentum) patterns, 99.2% were found either as half-strip or di-strip (low-momentum) patterns, and 0.8% were not found by the cathode LCT card. The differences in position between trigger and precision DAQ data are shown in Figure 11.14. The inefficiencies can be mostly eliminated in the future by inclusion of additional trigger patterns for tracks that travel very close to the boundary between half-strips or di-strips.

The second method for estimating the efficiency and resolution of the cathode LCT card used the silicon tracking telescope. This telescope defines tracks to an accuracy of about 100 µm after 100 cm extrapolation to the chamber. Half-strip cathode patterns were found for 96% of the

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**Fig. 11.12:** The 96-channel cathode Comparator cards used in the 1998 test beam studies. These receive amplified cathode signals from CFEBs on which they are mounted. Six Comparator ASICs produce 192 half-strip bits that are converted to differential LVDS for transmission to CLCT cards.
tracks, with position residuals very close to a box distribution one-half strip wide. Another 3.7% of tracks were found as di-strip patterns by the cathode LCT logic. The positions of these tracks in di-strip units shows that di-strip patterns occur at the boundaries between half-strips, where the half-strip pattern tables were not optimally tuned. Another 0.25% of tracks were not found by the cathode LCT logic. Again, the inefficiencies can be mostly eliminated by inclusion of additional trigger patterns for tracks that travel very close to the boundary between half-strips or di-strips where the pattern tables were not optimally tuned. The net cathode LCT efficiency is found to be 99.75±0.04% in this study.

The VME 9U-height LCT cards produced in 1999 are shown in Figure 11.15. These handle large numbers of front-end signals, due to the data compression in comparator ASICs as well as the use of Channel-Links. For this round of tests, the same hardware was used for cathodes and anodes, while the different algorithms were implemented using different PLD configurations. CLCT boards input signals from 480 strips, an entire chamber, while ALCT boards handled 192 wire groups, one half of a chamber. Input signals were received by Channel-Links and fed into a single Altera 10K200E PLD. Cathode and anode LCT boards differed only by the algorithms implemented in the PLDs. The LCT boards sent input bits and output LCTs to the DAQ system through a FIFO dump to a DAQ motherboard.

The ALCT version of the LCT99 module used the full envelope of wire groups shown in Figure 11.10. The CLCT version used the envelope shown in Figure 11.8 but with the edges at ±2 units trimmed. The different patterns within the envelope were not distinguished, but rather the number of layers hit within the envelope was counted. We anticipate the final version of CLCT/TMB boards will use this type of module, updated with larger gate arrays having the capacity to use more patterns.
11.9.3 Anode LCT Prototypes

In the 1998 tests, the anode discriminator output bits were sent to a 48-strip anode LCT card (see Figure 11.13), which identified the multi-layer patterns of valid muon trajectories and the bunch crossing. A mezzanine card converted LVDS signals to TTL levels. These signals were distributed by a “front” Altera 10K50 PLD to Cypress 128Kx8bit SRAMs. The SRAMs contained all possible patterns as LUTs. A “rear” Altera 10K20 PLD collected the patterns from the SRAMs and selected the best according to pattern number. Higher numbers corresponded to larger numbers of hit layers and straighter tracks. The CAMAC interface was implemented in another Altera 10K20 PLD.

For the anode LCT card, there are two efficiencies to be evaluated: wire pattern-finding, and bunch crossing identification. The wire pattern-finding efficiency was found by comparison of
the position of layer 3 TDC hits to the anode LCT position. It is found that 98.7% of tracks match exactly, 0.8% match within 1 wire group, 0.4% are further away, and 0.1% of events contain no
anode LCT pattern. If ±1 wire group matching is allowed, the overall anode LCT pattern finding is 99.5±0.1% efficient.

To find the bunch crossing efficiency, the anode LCT module uses an \( n \)-layer coincidence technique. At the test beam, the muons arrive asynchronously to the 40 MHz clock used by the synchronous electronics, unlike in the LHC conditions. The phase of the muon arrival was determined by using a TDC to measure the delay between a test beam muon scintillator paddle and the 40 MHz clock. The efficiency for correct bunch crossing identification depends on this phase. After choosing only test beam muons with phase within the ±2 ns specification for system timing accuracy, the bunch ID efficiencies are, for layer coincidence levels 1-6, 98.0%, 99.2%, 99.2%, 99.1%, 98.5%, and 98.0%, respectively. Optimal efficiency is found for coincidence levels 2, 3, and 4.

The dependence of ALCT bunch ID efficiency on background rate was studied at the GIF facility. The efficiency is above 99% up to the nominal maximum LHC rate of 20 kHz/wire group, dropping only slightly to about 98.5% at seven times the maximum rate (140 kHz). The implications for the CSC trigger system are important: the CSC Track Finder does not need to correlate muon stubs from apparently different bunch crossings, but can demand that all muon stubs arrive in the same bunch crossing. This represents a large simplification in the CSC Track Finder logic described in Chapter 12.

Based on the 1999 prototyping, we re-designed the system to save costs in cabling and PC boards. This required new anode electronics that are mounted on the chamber. A 384-channel third-generation anode LCT trigger and readout card, called ALCT2000 (shown in Figure 11.17), was built during early 2000. This prototype supplies anode triggering and readout for an entire CSC chamber. Five such modules were built in early 2000 and have been used in tests with cosmic rays at Fermilab. The new module incorporates additional features in support of the anode front-end boards, such as front-end amplifier test pulsing, temperature monitoring, and voltage and current self-monitoring [11.10].

A block diagram of the ALCT2000 board is shown in Figure 11.18. Anode data flows from left to right, starting with the discriminator output signals. These pass into custom delay/translator ASICs which allow a variable delay (0-30 ns in steps of 2 ns) to ensure correct phasing of the anode signals with respect to the board clock, and convert differential LVDS levels to TTL single-ended levels. The delayed signals are then fed to four 96-channel LCT PLDs that find wire patterns and output them to a single Concentrator PLD. The Concentrator PLD finds the best two LCT patterns and outputs them to Channel-Link bit serializers for transmission to the TMB and full data dump to the DAQMB. Analog functions are at the bottom of the diagram. The Altera PLDs are loaded from flash RAMs on power-up, and can be re-configured using one of the two JTAG chains. Another JTAG chain allows for quick re-configuration of registers that control common functions such as trigger configuration and AFEB discriminator thresholds, and read back currents, temperature, and thresholds.

The trigger features of the ALCT2000 prototype are separated into two types of PLDs. The LCT PLDs each handle 96 channels of anode input data. They perform a number of functions shown in Figure 11.19. On the left side are the external ADB cards and delay ASICs. Proceeding to the right are the functions for masking off hot anode channels, injecting test patterns, one-shots to stretch anode signals to allow coincidence with late-arriving hits, sharing necessary signals between gate arrays, calculating the number of anode planes with hits in the predetermined collision and accelerator patterns, and priority encoding to select the best LCTs. In addition, there
is a parallel DAQ data path for the raw anode hits, which are fed into a FIFO for readout under control of the Concentrator PLD.

The Concentrator PLD provides a number of functions: it finds the best two LCT patterns, outputs them to the TMB, and controls the LCT PLDs. A block diagram of this chip is shown in Figure 11.20.

11.9.4 TMB and CCB Prototypes

TMB and CCB prototypes were built for use in 1998 and 1999 test beam studies at CERN. These prototypes used Altera PLDs. The prototypes used in 1998 are shown in Figure 11.13. Signals were received by the TMB from ALCT and CLCT prototypes. Studies were complicated by the variable phase of the 40 MHz oscillator with respect to the test beam muons, which makes an accurate estimate of the time correlation efficiency impossible. Nonetheless, the tests showed a TMB efficiency of 98% for a ±1 bx time coincidence. This number should be higher with a synchronous beam. The prototypes built for the 1999 studies, shown in Figure 11.21, used VME form factors and implemented VME interfaces for ease of configuration.

Fig. 11.17: The “ALCT2000” module, a 384-channel on-chamber board incorporating trigger functions, pipelined raw data storage, and support of anode front-end boards.
11.9.5 MPC Prototype

The Muon Port Card prototype board built in 2000 receives data from up to three Trigger Motherboards (TMB99 prototypes), performs sorting of up to 3 best muons out of 18, and transmits data representing those best three muons to Sector Receiver (SR) board over six optical links. It was decided to interface with only three TMB99s in order to simplify the design of this first prototype. Subsequent prototypes will have the full input capacity. The prototype includes six HDMP-1022 G-Link serializers and six Methode MDX-19 optical modules for communication with one SR.

In addition to the main sorter logic, two groups of FIFO buffers are implemented to test the MPC internal logic and its communication with the Trigger Motherboards (TMB) over channel.
Fig. 11.19: Block diagram for logic contained in the 96-channel LCT PLDs on the ALCT2000 prototype.

Data communication was tested between the TMB and MPC by loading pass-through logic in the sorting PLD. LCTs were input from the TMB over Channel Links and then read back from the Port Card via the output FIFO over VME. The test was successful. In addition, the sorting logic was tested by load many millions of test patterns into the input FIFO and reading the results of the sorting logic from the output FIFO. This test was also successful. A more complete test of the CSC Track Finder system using the MPC, SR and SP together is described in chapter 12.

11.9.6 Radiation Resistance

The CMOS electronics used in the CSC Local Trigger is subject to two types of effects due to radiation [11.11]. The first effect is due to ionization of charged particles. This gives rise to cumulative charge build-up and defect activation effects in the silicon dioxide insulation layers that depends on the total ionizing dose (TID). The second effect is that of logic upsets that cause errors, particularly in memory-based devices such as programmable gate arrays and RAM chips. These are known as single event upsets (SEUs).

The total ionizing dose for 10 LHC years at full luminosity is expected to be no more than 1.7 krad at the inner CSC chambers and no more than 100 rad at the outer CSC chambers [11.12]. These numbers are far below the 10-30 krad tolerance of most CMOS devices. The integrated neutron flux is estimated to be no more than \(6 \times 10^{11} \text{ /cm}^2\) at the inner CSC chambers and no more than \(1.3 \times 10^{11} \text{ /cm}^2\) at the outer CSC chambers [11.12]. Our guideline is to take a factor of three safety factor on the neutron rate: a maximum integrated neutron flux of \(2 \times 10^{12} \text{ /cm}^2\) for...
on-chamber electronics and $4 \times 10^{11} / \text{cm}^2$ for electronics in the peripheral crates for $5 \times 10^7 \text{s}$ of running time.

All of the on-chamber CSC trigger electronics have been tested for radiation resistance [11.13][11.14] using 63 MeV proton beams at UC Davis, which give a well-calibrated TID dose and are expected to give SEU rates similar to the rates for neutrons from LHC collisions. No significant effects were seen due to TID within the expected dose on any devices. No problems were seen for the comparator ASICs.

Among ALCT components, the Altera PLDs show a strong SEU sensitivity. The PLDs can be periodically reloaded from Altera flash RAMs, which showed no SEUs. Reloading these devices takes about 150 ms. This refresh would be done using a central command, distributed
Tests have shown that if any bit flip is counted as an error, the cross-section is $2.3 \times 10^{-9} \text{ cm}^2$ per neutron: each chip will suffer an SEU every 3 hours at full throughput the TTC system [11.6].
luminosity (including the safety factor of 3). If only ALCT trigger errors are counted, the cross-
section decreases to $7 \times 10^{-11}$ cm$^2$.

In principle, the SEU problem can be greatly reduced by a design in which critical
ALCT logic is triplicated and a small “voting” circuit chooses the answer found by at least two of
the three circuits have found. This reduces the SEU problem to only those cases in which two
SEU’s have occurred within the same FPGA or PLD. According to Poisson statistics, this happens
with probability $P(2) = 0.5xP^2$, where $P$ is the probability of each SEU. Since $P$ is generally a small
number, $P(2)$ can be made extremely small. A refresh from flash RAMs at that time resets $P$ to zero,
and also fixes the rare cases in which the voting circuit itself undergoes an SEU. However, tests of
such a design have shown a cross section of $5 \times 10^{-11}$ cm$^2$, only modestly smaller than the non-voted
logic cross-section. One benefit of the voting technique is that the errors are internally detected and
the erroneous ALCT outputs are suppressed.

The periodic refresh cycle is also required for the CFEB Xilinx FPGAs, which show
SEU cross-sections in the range $1 \times 10^{-10}$ cm$^2$. These chips reload in about 5 ms. Currently,
conversion from Altera designs to Xilinx is being studied because of the much faster reload time.

Peripheral trigger electronics will be studied for radiation effects when the pre-
production prototypes become available.

### 11.10 Simulation Status and Results

In the ORCA reconstruction program (version 4), the CSC Local Trigger package
[11.15] implements each of the CSC Local Trigger modules and the trigger data passed from one
module to the next as classes. The CSC Local Trigger package simulates the trigger functionality
up to and including the Sector Receiver, and passes its results to the CSC Track Finder package.

The CSC Local Trigger package receives input from the CSC chamber simulation.
These ‘DIGIs’ are the software analogues to the outputs of the AFEB and CFEB boards. The anode
wire DIGIs contain the anode discriminator hits, and the cathode strip DIGIs contain the results of
the cathode strip preamplifiers and comparator ASICs (half-strip hits). Both anode and cathode
DIGIs contain timing information digitized in units of bunch crossings.

The classes for the ALCT, CLCT, TMB, MPC, and SR implement the patterns and logic
as previously described for the hardware. The four data classes in the CSC Local Trigger package
represent the connections from ALCT to TMB, from CLCT to TMB, from TMB to MPC, and the
SR output (to the CSC Sector Processor). Since the Muon Port Card only sorts the correlated LCTs
and adds a chamber ID, the class used for the data passed from TMB to MPC is also used for the
data passed from MPC to SR.

The efficiency of CLCT pattern-finding can be determined by recording the number of
chambers with CLCT stubs, given that an ALCT stub has been recorded for that chamber.
Likewise, the efficiency of ALCT pattern-finding is given by the fraction of chambers with ALCT
stubs, given that a CLCT stub has been found. If the stubs are required to lie within the chamber
struck by the generated high-momentum muon, the found efficiencies are nearly 100%. Since both
types of muon stubs are found with full efficiency, the combination is also fully efficient. The small
inefficiency is strongly dependant on the tails of the drift time distribution and the amplifier
response. Study of these effects is continuing [11.15].
In Figure 11.23 are shown the deviations between the $\phi$ position reconstructed by the CSC local trigger and the $\phi$ of the generated muon track. The deviations are shown for each muon station, in units of CSC Track Finder $\phi$ bins which are 0.26 milliradians wide. Since the CSC strips are radial, a constant resolution in strip widths corresponds to a constant resolution in the $\phi$ coordinate. The distributions are observed to be independent of radius, with only small tails. This is an indication that the deviation is essentially due to the one-half strip width granularity of the simple CLCT trigger algorithm used in the simulation. Future versions of CLCT boards may have larger FPGAs than current prototypes, that would allow them accommodate additional trigger patterns, thus improving the position resolution.

**Fig. 11.23:** The differences between the $\phi$ position reconstructed by the CSC local trigger and the $\phi$ of the generated muon track at layer 3 of the chambers. The differences are shown for each type of muon chamber in units of CSC Track Finder $\phi$ bins (0.26 milliradians).

The $\phi$ resolutions that are obtained by taking the RMS of the distributions within $3\sigma$ of the means are shown for each CSC station in milliradians in Figure 11.24. This resolution determines the ability of the CSC Track Finder to measure track curvature in the muon system,
which will be discussed in the following chapter. These resolutions correspond to 0.15 to 0.2 strip widths in ME1 and 0.125 to 0.17 strip widths in the other stations.

The next set of plots show deviations between the $\eta$ position reconstructed by the CSC local trigger and the $\eta$ of the generated muon track, for each muon station. In Figure 11.25, the deviation is shown in units of $\eta$ bins at the input of the CSC Track Finder, which are 0.025 units of pseudorapidity. This binning is wider than the intrinsic resolution of about one wire group, but has been shown to be sufficient for all CSC track finding purposes. In most cases, the distribution lies well within one $\eta$ bin width.

Note that the $\eta$ resolutions in ME1/A and ME1/1 are not quite ideal. This is due to the 25° tilt of the anode wires in that chamber, which is confirmed by Figure 11.26 (right). There is also a bowed appearance to the plots of the 20° wide chambers (ME2/1, ME3/1, and ME4/1) in Figure 11.26 (left). This effect is due to the difference in $\eta$ for a given wire between the center of the chamber and the edge: the wire is stretched straight, while the line of constant $\eta$ is an arc of a circle. The $\eta$ resolution, shown in Figure 11.27, is obtained by taking the RMS of the distributions within $3\sigma$ of the mean values. The resolution is almost constant at 0.007 units.

Fig. 11.24: RMS differences between the $\phi$ position reconstructed by the CSC local trigger and the $\phi$ of the generated muon track. The differences are shown for each CSC station as a function of pseudorapidity, in units of milliradians.
11.11 Maintenance and Operation

We plan to have spare boards and components sufficient for 10 years of LHC operations. Each board will have a JTAG- or VME-readable register that labels the particular trigger configuration that was loaded into the board. The entire set of LUT contents and FPGA programs will be given one unique identifier. There are many FPGAs and LUTs in the design, so it is important to verify that the correct patterns were loaded. We do not foresee generating LUT contents on the boards from a VME-loadable register. Rather, we will have precompiled FPGA programs (and LUT contents) that are certified to work properly and that meet all timing specifications.

Fig. 11.25: The differences between the $\eta$ position reconstructed by the CSC local trigger and the $\eta$ of the generated muon tracks. The differences are shown for each type of muon chamber in units of $\eta$ bins (0.025 units).
Fig. 11.26: Differences between $\eta$ reconstructed by the CSC local trigger and $\eta$ of the generated muon track. These are shown for ME1/1 (left) and ME3/1 (right) versus strip number, in units of $\eta$ bins (0.025 units).

Fig. 11.27: The RMS difference between the $\eta$ position reconstructed by the CSC local trigger and the $\eta$ of the generated muon track. This is shown for each type of muon chamber, as a function of pseudorapidity, in absolute units.
11.12 Status and Schedule

The CSC trigger development schedule is shown in Figure 11.28.

Near-final prototypes and radiation test results exist for all on-chamber CSC system electronics, *i.e.*, the CFEB, AFEB, and ALCT boards. The on-chamber boards will be produced on a time scale similar to that for the CSC chambers, so that electronics may be mounted semi-permanently on the chambers soon after the time of production for testing. Orders for production of on-chamber CSC system ASICs, including the Comparator chip, will be placed in early 2001. Production of on-chamber boards will commence later in 2001. Production and testing of these boards will take about two years.

Off-chamber CSC local trigger-related electronics, *i.e.*, CLCT/TMB, MPC, DAQMB, and CCB boards, have been successfully prototyped but not finalized. It is anticipated to begin production mode of these boards in 2002, about a year later than the on-chamber CSC electronics. Production and testing of these boards will take about two years.

The installation schedule for the CSC Local Trigger calls for on-chamber electronics to be installed as the electronics are checked out, so that chambers and electronics can be tested, shipped to CERN, and mounted as a single unit. Peripheral crate electronics will be installed at CERN starting in 2003 and will be completed by the middle of 2004 in order to perform integration with other elements of the trigger and DAQ, and to allow sufficient time for system tests. This
schedule is dependant on a timely completion of electrical, cooling, rack, and safety support services on the periphery of the endcap iron disks in the collision hall and the counting room.

References


